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Transilvania University of Brasov

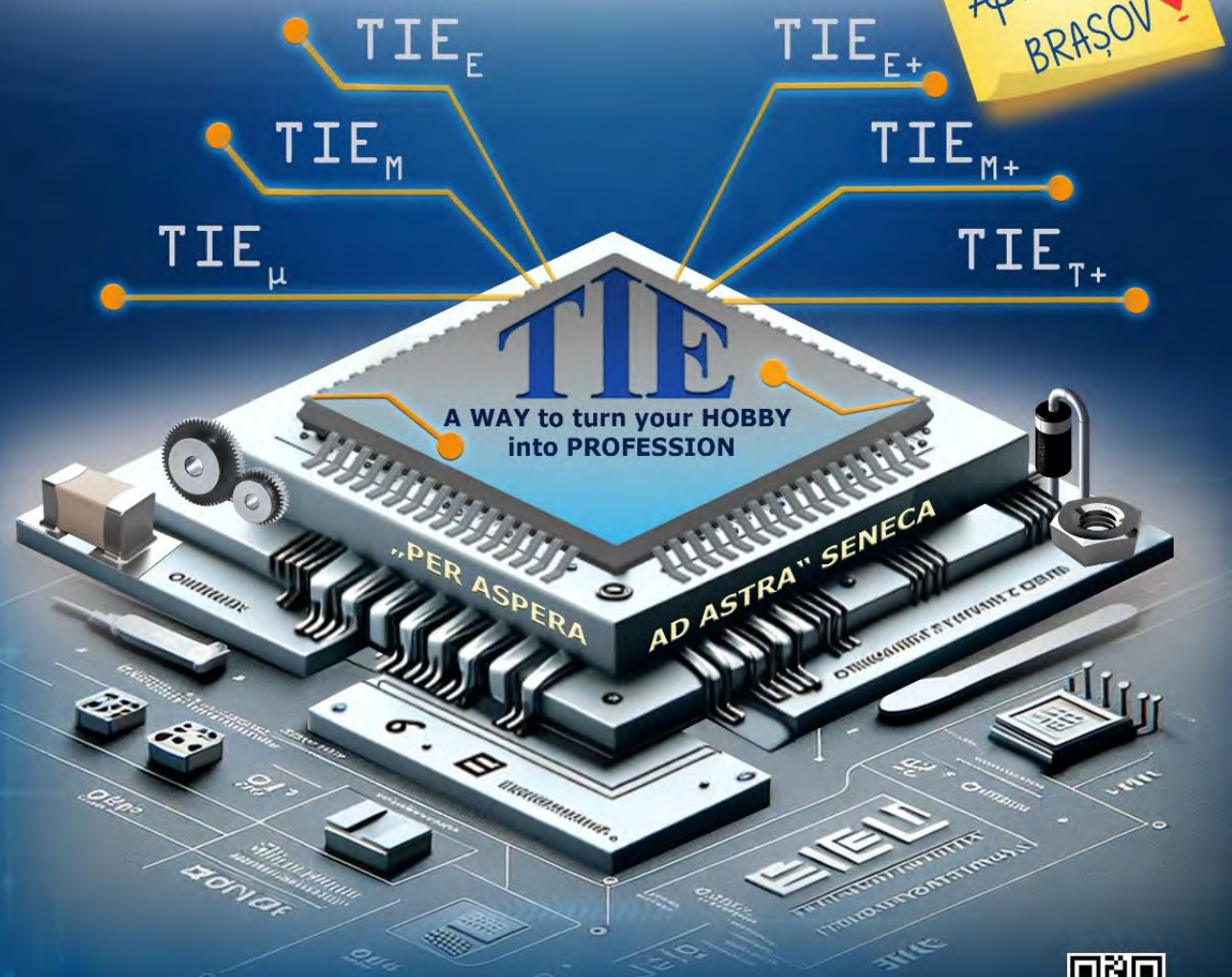
TECHNICAL UNIVERSITY OF CLUJ-NAPOCA ROMANIA

APTE
Association for Promoting Electronics Technology

# TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS

## Industry-wide Student Challenges

2nd - 5th April 2025
BRAȘOV

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TECHNOLOGIES of
INTERCONNECTIONS in
ELECTRONICS
Industry-wide
Student Challenges

*A WAY to turn your HOBBY into PROFESSION*

# TECHNOLOGIES OF INTERCONNECTIONS IN ELECTRONICS

## INDUSTRY-WIDE STUDENT CHALLENGES

## 34th Edition

**Transilvania University of Brașov,**

**April, 02 – 05, 2025**

# TECHNOLOGIES OF INTERCONNECTIONS IN ELECTRONICS – 2025
# INDUSTRY-WIDE STUDENT CHALLENGES
## Program Brochure


**Welcome to TIE 2025 Event ..... 1**
**Event Committees 2025 ..... 17**
TIE 2025 Event Agenda ..... 20
**TIE & TIE$_M$ & TIE$_{PLUS}$ past, present and future editions ..... 27**
Workshop Program ..... 29
**Workshop ADR Centru (EEN) ..... 31**
Wednesday, April 2 Program ..... 37
**TIE$_{Eplus}$ Contest ..... 39**
Thursday, April 3 TIE$_{MPLUS}$, TIE$_{TPLUS}$, TIEμ Program ..... 44
**TIE$_{MPLUS}$ Contest ..... 45**
**TIE$_{TPLUS}$ Contest ..... 49**
**TIEμ Contest ..... 53**
Thursday, April 3 MICROELECTRONICS DAYS Program ..... 57
**Dr. Christian VON ALBRICHSFELD** ..... 59
Addressing semiconductor talent gap: research on industry skills needs, **Victoria CUMMINGS** ..... 60
Introduction to Package Design and Analysis, **Carolyn TUBILLO** ..... 61
Friday, April 4 MICROELECTRONICS DAYS Program ..... 62
European Chips Skills Academy, **Victoria CUMMINGS** ..... 64
Silicon-to-Systems: Path towards Next Generation Design, **Dr. Peter TRANITZ** ..... 65
Friday, April 4 TIE$_E$, TIE$_M$ Program ..... 66
**TIE$_E$ Contest ..... 67**
TIE Certificate for recognition by the industry of students competence in PCB design ..... 71
TIE$_E$ Committees ..... 72
TIE Winners ..... 74
TIE$_E$ 2025 Participants ..... 76
**TIE$_M$ Contest ..... 89**
TIE$_M$ Committees ..... 93
TIE$_M$ Participants ..... 94
**Industry ..... 99**
**Research ..... 111**
**WELCOMES TO TIE 2026 ..... 116**

**Welcomes to TIE 2025 Event**

# Dear Participants of TIE 2025,

We warmly welcome all TIE participants to this event, which is dedicated to training and validating future professionals in the field of electronic packaging.

TIE provides a platform where students are challenged to address real-world issues in the electronics industry, specifically in electronic packaging, a crucial aspect of the design and production of electronic products. In this context, the collaboration between academia, responsible for educating and training future engineers, and industry, the direct beneficiary of these graduates, forms a high-performance ecosystem. This partnership ensures mutual benefits: students gain access to highly qualified jobs, the industry recruits well-trained engineers, and academic staff can effectively tailor curricula to meet the evolving needs of the sector.

The challenges presented at TIE 2025 consist of six topics, developed by industry professionals in collaboration with academic experts, for students to solve. These topics reflect various challenges encountered in electronic product design.

The current edition focuses on three electrical topics: designing a medium-complexity PCB, evaluating the signal integrity and power behavior of an interconnection structure, and designing the interconnection within a System-in-Package (SiP). Additionally, three non-electrical topics cover optimizing the mechanical design of an electronic product, assessing its response to mechanical stress, shocks, and vibrations, and evaluating its thermal behavior and management. The challenges are supported by industry-leading software solutions, including advanced tools for mechanical design and thermal analysis. These software solutions enable students to simulate and optimize their designs with high accuracy, enhancing their learning experience.

The complexity and success of TIE would not have reached its current level without the significant involvement of all participants, industry professionals, academic staff, and, most importantly, the enthusiastic students who seize this opportunity to demonstrate their skills and creativity.

We also extend our gratitude to the companies that have provided essential modeling and simulation licenses. Specially, we would like to acknowledge **Cadence** offering over 30 licenses for TIE micro, made available to the organizers for an entire year, along with the necessary technical support. This generous contribution has been a key factor in the success of TIE 2025.

## Welcomes to TIE 2025 Event

A special thank you goes to all the volunteers—over 70 of them—who have dedicated their time and effort to ensuring the best organizational and technical conditions for the event. We also deeply appreciate the support of our sponsors, whose financial contributions have made it possible to host TIE 2025 under excellent conditions.

Finally, we must highlight the invaluable involvement of **Transilvania University of Brașov** and the **Regional Development Agency Centru** in creating the welcoming and family-like atmosphere that defines TIE. This event has truly become the **spring convention of the electronic packaging community** in this part of Europe.

We wish all participants a pleasant and productive stay in **Brașov, Romania!**

**Prof. D.H.C. mult. Paul SVASTA, Ph.D.**
National University of Science and Technology
POLITEHNICA of Bucharest, Romania
APTE-Association for Promoting Electronics Technology
TIE General Chair

**Prof. Ovidiu POP, Ph.D.**
Technical University of Cluj-Napoca
TIE General Co-Chair

**Welcomes to TIE 2025 Event**

# Dear participants and guests,

On behalf of the local organizing committee, we are delighted to welcome you to Brașov for the 2025 edition of the Technologies of Interconnection in Electronics (TIE) event. By organizing Romania's first Microelectronics Day, Transilvania University of Brașov highlights its commitment to current technological advancements and its vision for the future, with microelectronics playing a key role.

Building on the region's rich scientific, industrial, and cultural traditions, Transilvania University of Brașov has a longstanding history of participating in TIE events, while local industrial partners continue to expand their presence in electronics, digital design, and verification.

Returning to Brașov after more than a decade, the event has expanded to 6 student challenges covering different aspects of electronic packaging: 34$^{th}$ edition of the classic PCB design challenge $TIE_E$, the 4$^{th}$ edition of $TIE_M$ for mechanical design, the 9$^{th}$ edition of the advanced analysis $TIE_{EPLUS}$, the 3$^{rd}$ edition of $TIE_{MPLUS}$, the 3$^{rd}$ edition of for $TIE_{TPLUS}$ (thermal) and second edition for TIEμ (micro).

TIE is an established student challenge, a proven path for students to get hands-on experience with hot industry topics such as chiplets and advanced packaging. Furthermore, students get access to state-of-the-art EDA tools, trainings and documentation.

We are looking forward to meeting you in Brașov for a great TIE 2025!

**Prof. Titus Constantin BĂLAN, Ph.D.**
Dean of the Faculty of Electrical Engineering and Computer Science
Transilvania University of Brașov
TIE 2025 Chair

**Assoc. Prof. Cătălin CIOBANU, PhD**
Coordinator of the Smart Electronic Systems Research Center
Transilvania University of Brașov
TIE 2025 Co-Chair

# TIE – a Best Practices for the Romanian Universities Contribution to Microelectronics Value Chain in Europe

Modern life heavily relies on mobility, communication, smart environments for living and working, and gadgets for entertainment and health. Smart devices can enhance our senses, understand and anticipate our needs, communicate securely, and act quickly and safely. Their evolution towards greater intelligence is unstoppable. All these devices are powered by semiconductors, which integrate an increasing number of transistors, now approaching atomic dimensions.

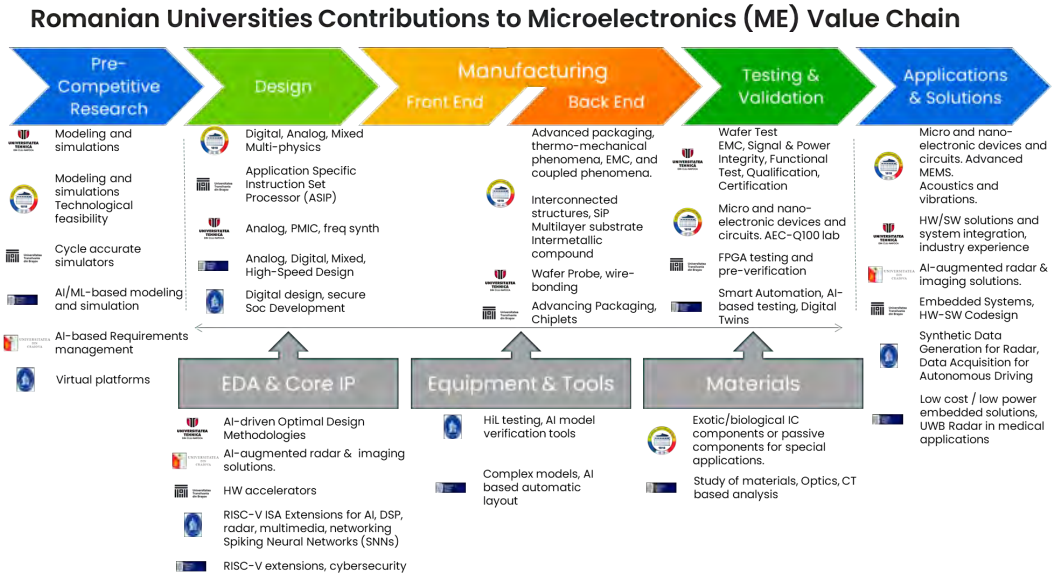
The global semiconductor market surpassed $550 billion in 20231. Europe accounts for less than 10% of this market2. In 2023, the Council of the European Union approved the Chips Act, aiming to invest €43 billion to double Europe's share of global semiconductor production to 20% by 2030. The current geopolitical situation highlights the need for Europe to build its own defense system, which relies on semiconductor sovereignty.

We are facing a significant technology gap between Europe, Asia, and America. In my opinion, the biggest challenge we must address at both the European and national levels is developing a qualified workforce capable of developing the microelectronics value chain. The United States began reducing its semiconductor manufacturing footprint when DRAM production was transferred to Japan. Later, TSMC (Taiwan Semiconductor Manufacturing Company) emerged, gradually taking over and advancing the most sophisticated semiconductor technologies3. The United States and Europe retained only the design of increasingly complex devices, design tools, and EUV lithography machinery. Now, it is time to work diligently to close this gap.

In Romania, in the early '90s, all investment in microelectronics was halted, and university programs underwent continuous restructuring of their curricula. However, in Romanian universities, there were faculty collectives that continued to maintain relevant curricula for the microelectronics value chain and elevate the scientific and technological standards. They leveraged opportunities such as educational exchanges, European grants, and industry research projects to build laboratories and conduct significant research. The results of these efforts were utilized to improve and upgrade courses.

Based on my personal research, made possible through NXP Semiconductors Romania's participation in IPCEI ME/CT (https://ipcei-me-ct.eu/), in collaboration with six universities in Romania4, I identified the mapping of competencies presented in Figure 1

[1] Source: https://investors.nxp.com/static-files/8e7721d4-bf71-493b-b4d6-e179214de061
[2] Source: https://www.eusemiconductors.eu/sites/default/files/ESIA_WSTS_PR_2212.pdf
[3] Taiwan began ramping up skills in microelectronics in 70s. More details here: https://en.wikipedia.org/wiki/Semiconductor_industry_in_Taiwan
[4] In IPCEI ME/CT, NXP Semiconductors Romania collaborates with the following universities: Universitatea de Știință și Tehnologie Politehnica București (UPB), Universitatea Politehnica Timișoara (UPT), Universitatea Tehnică din Cluj Napoca (UTCN). Universitatea Tehnică Gheorghe Asachi din Iași (UTIS), Universitatea Transilvania din Brașov (UTBV), Universitatea din Craiova (UCV). Only them are reflected in Figure 1




Besides the universities reflected in this figure, it is worth to mention that Universitatea Lucian Blaga din Sibiu, Universitatea „Ștefan cel Mare” din Suceava, Universitatea „Dunărea de Jos” din Galați also maintain and train important competencies for the Microelectronics Value Chain.

These universities collaborate with the industry to organize the annual TIE (Technologies of Interconnection in Electronics) student contest, which has been running for over 30 years and is likely the longest and most important electronics contest in Europe. Participants are challenged to learn, experiment, and achieve results in six areas of electronics interconnections: PCB design ($TIE_E$), signal and power integrity ($TIE_{EPLUS}$), mechanical design of electronic packages ($TIE_M$), structural and thermal management analysis ($TIE_{MPLUS}$), thermal management optimization ($TIE_{TPLUS}$), and system-in-package design (TIEμ). So far, more than 3,000 students have participated, with over 1,500 successfully completing the competition and receiving industry-certified diplomas.

Romania is one of the largest countries in Europe. We have strong universities with over 10,000 students in electronics and more than 13,000 students in computer science, along with significant research capabilities. Major semiconductor companies such as NXP Semiconductors, Infineon, Microchip, Continental, and Bosch are present in Romania. We have the potential to expand the microelectronics industry in Romania, offering growth opportunities for companies and making a substantial impact on developing Europe's sovereignty in semiconductors and related industries.

**Radu PREDA,**

Manager of Partnerships under Subsidy Projects,

NXP Semiconductors Romania

# TIE 2025

What is TIE today? Today TIE is more than just an academic competition, it is the platform that brings together industry and academia to create the premises, the opportunity to share, to experience the real challenges that new technologies bring to this hyper-dynamic field.

The close collaboration between academia and industry offers future engineers the opportunity to improve, evaluate and validate the theoretical and applied aspects acquired during their university studies as well as those specific to the engineering profession.

Each stage of the competition is an opportunity to learn, develop skills and gain valuable feedback, highlighting its role as a link between academic knowledge and its practical application in the professional field.

The permanent technological progress of the companies involved in research, design, development of both CAD/EDA concepts and top of the range products has required TIE to reinvent itself year after year, to reorganize itself.

Today, TIE is a mature platform that brings together both electrical/electronic ($TIE_E$, $TIE_{EPLUS}$, TIEμ) and non-electrical ($TIE_M$, $TIE_{MPLUS}$, $TIE_{TPLUS}$) aspects, covering the whole multidisciplinary spectrum of processes.

The TIE community acts as an engine for science, technology, advanced manufacturing, promotes the development of education.

I am pleased to note that the fruitful, sometimes contradictory, discussions during the sessions organized under the auspices of the TIE have led to profound changes, in terms of subject descriptions, teaching portfolios and even the development of new training methods in which the applied learning component is a priority.

Moreover, I observe that this impactful, hyper-competitive field such as electronic systems development and applications is pushing to the maximum the massive integration of available design resources such that the design constraints, robustness, reliability, cost and technological limitations encountered not so long ago have been successfully overcome.

The course of this scientific event leads me to believe that in future TIE editions we will also find competition sessions dedicated to processor design, parallel design, concurrent integration, etc.

Finally, I would like to express my thanks to all those involved in the organization of the current edition of TIE, sponsors and exhibitors, whose contribution has been essential to maintain a high level of quality.

**Lecturer Marius CARP, Ph.D.**
Transilvania University of Brașov
$TIE_E$ Technical Committee – Academic Trainer

# Preface $TIE_M$

The student contest named Technologies of Interconnections in Electronics, Mechanical concept ($TIE_M$) involved a great number of participants, graduated students, in the last five years. It is a big challenge and an opportunity to evaluate the knowledge acquired during four years of study and moreover the passion of participants for computer aided design in this interdisciplinary field implying mechatronics and electronics. It is a contest where the mechatronics students are working near their colleagues studying electronics. As we know, the Electronics Packaging, the Design for the Future, has been one of the most important research activities in our university since 2019 implying teachers, researchers as well as students and young engineers.

Since the beginning it was a great success due to the company's involvement, such as Continental Timișoara, Continental Sibiu that are interested in testing and pointing out the solutions discovered by the students, when some practice problems should be solved. The requirements are testing, refrigeration and thermal evolution during functioning, manufacturing and applying the design principles for all of these. The teams are evaluated by the experienced engineers working in the company and by the teachers, other than from the university the students come from. Finally, only the best students are rewarded, but all of them have achieved a new step, their satisfaction with finding out a passion, which could be for long time and could be in continuous evolution, so it is a great success for them, for teachers and for the contest committee.

We aim to improve this activity and to turn it into a hobby for the students and young engineers, following the idea of competition approved by companies and universities.

**Lecturer Alina SPÂNU, Ph.D.**
POLITEHNICA Bucharest
$TIE_M$ Technical Committee – Academic Trainer

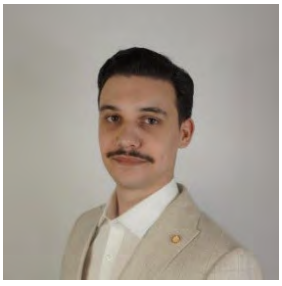
# $TIE_M$, $TIE_{MPLUS}$, and $TIE_{TPLUS}$ competitions

The $TIE_M$, $TIE_{MPLUS}$, and $TIE_{TPLUS}$ competitions play a critical role in uniting academic and industrial partners by offering a realistic simulation of the challenges encountered in the design, development, and validation of electronic modules. These events serve not only as a testing ground for theoretical knowledge but also as a platform where practical skills and innovative solutions are developed and refined.

In the $TIE_M$ contest, participants are tasked with developing a robust mechanical design for electronic modules within a constrained four-hour timeframe. This aspect of the competition mirrors the time-sensitive decision-making process found in professional environments and underscores the importance of efficient problem-solving and rigorous design methodology. It provides students with firsthand experience in applying classroom concepts to real-world scenarios, while simultaneously offering industry professionals a glimpse into the emerging talent and novel approaches that could shape future advancements.

The advanced simulation challenges, $TIE_{MPLUS}$ and $TIE_{TPLUS}$, further enhance the educational and practical value of the contests by introducing structural analysis and thermal management into the equation. These simulations are crucial for validating design integrity and ensuring product reliability under operational stresses. The extended preparation period, supplemented by expert-led workshops, allows participants to delve deeply into the mechanics of material behavior and thermal dynamics. For academic institutions, these exercises integrate computational methods with traditional engineering education, while for industrial partners, they reflect the rigorous procedures essential for product quality assurance.

Overall, the structured approach of these competitions provides a comprehensive overview of the developmental challenges associated with electronic module design and validation. The process emphasizes the significance of interdisciplinary collaboration, iterative improvement, and early error detection, all of which are vital to successful product development. By bridging the gap between theoretical instruction and practical application, the TIE series of events not only cultivates a more capable future workforce but also fosters a productive dialogue between academia and industry, ultimately driving innovation and ensuring that modern engineering practices meet the evolving demands of the market.



**Philip COANDĂ, Ph.D.**
Continental Automotive Timişoara
$TIE_{TPLUS}$ Co-Chair, $TIE_{MPLUS}$ Committees

# $TIE_{TPLUS}$ Contest: Academic Growth and Real-World Skills in Thermodynamic Simulation

The $TIE_{TPLUS}$ contest is a unique opportunity for students passionate about electronic engineering and thermal simulation of electronic equipment. It focuses on using computer-aided thermodynamic simulations (CAE) to analyze and improve the thermal performance of electronic systems. By applying advanced numerical methods, participants not only sharpen essential technical skills but also prepare themselves for the challenges of today's technology-driven industries.

### Why Thermodynamic CAE Simulations Matter

In modern engineering, thermodynamic Computer-Aided Engineering (CAE) simulations are a key tool for designing and optimizing technical components. They allow engineers to examine temperature distribution and heat flow in detail, helping to predict how heat will affect the performance and reliability of electronic equipment. Using methods such as Finite Element Analysis (FEA) and the Finite Volume Method (FVM), engineers can tackle real-world challenges in industries like electronics, automotive, aerospace and energy, where effective thermal management is critical.

As part of the $TIE_{TPLUS}$ contest, students are tasked with running an advanced thermodynamic CAE simulation of an electronic product. They explore both natural convection and forced conduction scenarios, giving them hands-on experience with fundamental thermal management principles. This directly helps prevent overheating and improves the efficiency and reliability of electronic systems.

### Real Benefits for Students and Future Career

$TIE_{TPLUS}$ is more than just a competition — it's a platform for personal and professional growth. Students put their theoretical knowledge to the test while gaining valuable practical experience with modern CAE software widely used in industry. Beyond technical skills, the contest strengthens problem-solving abilities, critical thinking, and analytical reasoning — qualities highly sought after by employers.

One of the key components of the contest is writing a detailed technical report based on the simulations. This not only deepens your understanding of thermodynamic phenomena but also improves the ability to communicate technical findings clearly and effectively — a crucial skill for any engineering career.

**Bridging Academia and Industry**

What makes $TIE_{TPLUS}$ stand out is its strong connection to the professional world, especially through its collaboration with Continental, a leading global company. This partnership helps bridge the gap between university and industry. Students gain insight into real industrial challenges, while companies benefit from fresh perspectives and well-prepared future engineers.

$TIE_{TPLUS}$ is an excellent opportunity to combine academic knowledge with real-world applications, opening doors to successful careers in electronic engineering and beyond. Whether students aim for a career in R&D, design, or system optimization, this contest helps them to stand out.

**Asoc. Prof. Cristian-Marcel FĂRCAŞ, Ph.D.**
Technical University of Cluj-Napoca
$TIE_{TPLUS}$ Technical Committee – Academic Trainers Chair

# The Technologies of Interconnection in Electronics (TIE) Industry wide student challenges: From Inspiration to Leadership in Packaging Design

The Technologies of Interconnection in Electronics (TIE) has been a cornerstone of my career, starting as a participant and eventually leading me to my current role as a Senior Packaging Engineer at a stealth company. As someone who has worked in various capacities, including Packaging Engineer at eSilicon and Inphi and Packaging Director at Marvell, I've seen firsthand how critical semiconductor packaging is to the development of modern electronics. TIE served as the initial source of inspiration for my journey into packaging engineering, and it continues to guide my work today as I help lead the technical committee for the contest.

**The Role of TIE in Shaping My Career Path**

My journey in packaging engineering started with TIE, where I was introduced to the complexities of interconnect design. The hands-on experience of designing functional interconnects and solving real-world design challenges fueled my passion for the field and shaped my career trajectory.

1. **Early Career:** TIE introduced me to interconnect design, laying the foundation for my work at eSilicon and Inphi, where I focused on power integrity, signal integrity, and electrical performance.
2. **Leadership at Marvell:** As Packaging Director at Marvell, I led teams developing high-performance packaging solutions, applying TIE's principles to balance trade-offs in size, speed, power, and integrity.
3. **Current Role:** Now as Senior Packaging Engineer, I tackle next-gen packaging challenges in miniaturization and power integrity, with TIE's lessons still guiding my work.

Through my work on the technical committee, I now strive to provide that same inspiration to future generations of engineers. I understand the impact TIE can have on shaping students' careers, just as it did mine.

**The Importance of Packaging in Modern Electronics**

Semiconductor packaging is crucial for device performance, impacting signal integrity, power integrity, and power efficiency. These areas are core to the challenges faced in TIE:

1. Power Integrity: Packaging must ensure that power delivery is stable and efficient to maintain optimal performance, a key issue TIE participants address.
2. Signal Integrity: Maintaining the integrity of electrical signals in increasingly miniaturized circuits is another challenge participants work on, similar to my current role.
3. Custom Layout: TIE participants work on custom layout techniques, designing tailored solutions for packaging challenges. These designs push the boundaries of what is possible in semiconductor packaging.

**How TIE Empowers the Next Generation of Packaging Engineers**

As a former TIE participant and now a leader on the technical committee, I can attest to the unique value of the contest. TIE serves as a platform not only for honing technical skills but also for developing a deep understanding of how packaging directly impacts the success of modern devices. Through TIE, students are exposed to the kinds of real-world challenges that I face daily in my career, making it an invaluable experience for anyone interested in packaging engineering.

1. Hands-On Design Experience: The challenges in TIE mirror the real-world problems packaging engineers must solve. Students must take into account thermal management, electrical performance, cost constraints, and manufacturing processes. These experiences prepare participants for the complexities of the packaging industry, where every design decision can have far-reaching consequences on performance and cost.
2. Networking and Industry Collaboration: TIE offers students the chance to interact with professionals in the packaging industry, providing exposure to cutting-edge tools, technologies, and best practices. As part of the technical committee, I ensure that students are connected with leading experts who can offer guidance and mentorship, furthering their development as future packaging engineers.
3. Encouraging Innovation and Problem Solving: The TIE contest encourages participants to think creatively, coming up with new ways to solve traditional packaging challenges. The industry is rapidly evolving, and the best solutions often come from unexpected places. I've seen firsthand how TIE participants' innovative approaches can lead to breakthroughs, pushing the boundaries of what's possible in semiconductor packaging.

**Conclusion: TIE as the Starting Point for a Career in Packaging Engineering**

The TIE contest is more than just a competition - it's a catalyst for the next generation of packaging engineers. For me, TIE was the spark that ignited my passion for semiconductor packaging, and it continues to inspire my work. The skills I developed through TIE set the foundation for my career in packaging.

As a member of the technical committee, I am excited to see how TIE participants will continue to innovate and shape the future of semiconductor packaging. For students in TIE, remember that the skills and knowledge you gain today will serve as the cornerstone for your future career in the ever-evolving field of packaging engineering. The work you do in TIE could be the next step in the future of electronics, and I look forward to seeing the breakthroughs you will create.

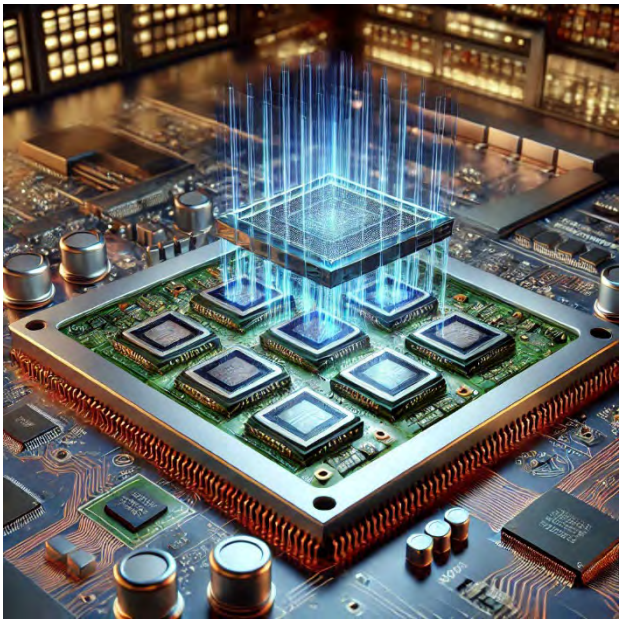
**Dan MANOLESCU**
APTE-Association for Promoting Electronics Technology
TIEμ Technical Committee Chair

# TIEμ 2025 - second edition industry-wide student challenge

The beginning of 2025 marked my return to the **TIE family**, an opportunity I deeply cherish. My journey with the **TIE (Interconnection Techniques in Electronics) student contest** began in 2007 when I participated as a student in this prestigious competition, which aims to promote **technological computer-aided design (CAE-CAD-CAM) of electronic modules** among students.

Over the years, TIE has evolved beyond its initial **$TIE_E$** category, expanding to include **$TIE_{EPLUS}$, $TIE_M$, and $TIE_T$**. Since last year, the competition has further broadened its focus by introducing **TIEμ (Micro)** — a premier student contest dedicated to **microelectronics, advanced packaging, and electronic module design**, emphasizing **System-in-Package (SiP) technologies**.

With the rapid advancement of semiconductor technology, the demand for **smaller, faster, and more efficient** electronic devices has never been greater. **TIEμ** provides students with a unique platform to **apply theoretical knowledge, refine practical skills, and push the boundaries of electronic packaging design**. The competition fosters **innovation, technical excellence, and collaboration** between students, academia, and industry leaders.



By participating in **TIEμ**, students gain **hands-on experience**, showcase their expertise in **microelectronics**, and contribute to the future of **high-performance, compact electronic systems**. Whether addressing **power integrity challenges, enhancing signal integrity, or optimizing designs for manufacturability**, TIEμ participants play a crucial role in **shaping the next generation of electronics**.

**Lecturer Raul FIZESAN, Ph.D.**
Technical University of Cluj-Napoca
TIEμ International Modelling & Simulation Environment Coordinator

# TIE - Life -changing experience

TIE experience represents a unique opportunity for participating students to validate their knowledge and skills to design electronic modules, in accordance with the real needs of the industry. Thus, the student has the chance to self-evaluate his professional level and, at the same time, he is able to predict the technical discussion topics from a future recruitment process. This is due to the fact that the contest subject is 100% oriented towards applicability and up-to-date engineering requirements. The experience of working under competitive pressure enriches the student's portfolio of lessons learned. I have summarized below, from the multitude of valuable lessons learned, two unique experiences I encountered at TIE:

1. Time relativity. I have always been passionate about science and have shown a lot of interest and curiosity about how things work around me, but I never imagined that I would understand what the concept of time relativity means by participating in TIE. How come? From the moment I received the TIE subject, I simply detach from everything that was happening around me. Four hours I managed to stay focused on solving the topic. I didn't see that somebody came and took pictures, I didn't even notice who was the competitor in front of me or that at some point he got up and left the room because his CAD tool encountered a "system crash". It was the most intense experience of perceiving time until then and I didn't feel it in any other competition or exam. Certainly for the evaluators and staff it was a long four hours journey, but we, the participants, felt that seconds turned into milliseconds and time flew by, giving the impression that it does not obey the same physical laws. After this unique experience, I felt that I could have given meditations on the relativity of time even to physics professor.

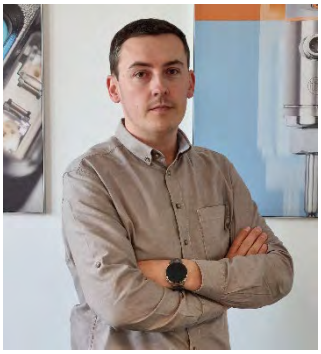
2. Ctrl+S... trivial, right? On my second participation in the competition (Sibiu 2012), I've learned a new lesson that I will never forget. In the pre-competition period, we were training with our mentor Adrian Petrariu, who used to say often: Save your layout progress! Don't forget to save your work! A good advice… For me, the stakes were high because a year before I had taken 2nd place and I wanted to surpass myself by aiming for 1st place. It was still the first edition where I participated in with a different CAD tool... and the inevitable happened: after 3 contest hours, while I was routing USB differential pairs, the image on the display froze and my laptop stopped responding to any command… software crash. My universe collapsed knowing that I hadn't saved anything on the layout side, and the CAD tool had no intermediate save option. Thus, I took the 12th place, but that experience helped me to avoid major inconveniences in my career as a design engineer. Create versions, constantly save the progress of your work!

## Welcomes to TIE 2025 Event

It is undeniable that innovations in the field of electronics/micro-electronics can change a nation destiny, in the current global context. But the innovation process in this field is not efficient and sustainable without close collaboration between university educational centers and industry. Through TIE, 33 years ago, the foundations of this bridge was laid with the enormous contribution of the TIE People (committee, members, consultants, professors, volunteers, students and sponsors), making this event a benchmark. An international benchmark in the field of professional electronics capable to inspire other fields of engineering and beyond.

I wish the best of luck to all TIE 2025 participants!

**Dorin ANTONOVICI**
Director Development
ifm prover s.r.l.
TIEμ - Industrial Committee Member



# Event Committees 2025

**Steering Committee**
**General Chairs:**
Paul SVASTA, POLITEHNICA of Bucharest; Association for Promoting Electronics Technology
Ovidiu POP, Technical University of Cluj-Napoca
**General Academic Co-Chairs:**
Dan PITICĂ, Technical University of Cluj-Napoca
Norocel CODREANU, POLITEHNICA of Bucharest
**General Industrial Co-Chair:**
Cosmin MOISĂ, Continental Automotive, Timişoara
**Financial Chair:**
Alexandru VASILE, POLITEHNICA of Bucharest
**TIE 2025 Chair:**
Titus BĂLAN, Transilvania University of Brașov
**TIE 2025 Co-Chair:**
Cătălin CIOBANU, Transilvania University of Brașov
**Steering Committee Members**:
Dorel AIORDĂCHIOAIE, Dunărea de Jos University of Galaţi
Alexandru BORCEA, Romanian Association for Electronic and Software Industry
Radu BOZOMITU, Gh. Asachi Technical University of Iaşi
Vlad CEHAN, Gh. Asachi Technical University of Iaşi
Gabriel CHINDRIŞ, Technical University of Cluj-Napoca
Cătălin CIOBANU, Transilvania University of Braşov
Philip COANDĂ, Continental Automotive Timişoara
Eugen COCA, Ştefan cel Mare University of Suceava
Daniel COMEAGĂ, POLITEHNICA of Bucharest
Mircea-Cătălin CONSTANTINESCU, University of Craiova
Aurelia FLOREA, Miele Brașov
Aurel GONTEAN, Politehnica University of Timişoara
Tecla GORAŞ, Gh. Asachi Technical University of Iaşi
Georgiana GOTIA, Continental Automotive Systems Sibiu
Ciprian IONESCU, POLITEHNICA of Bucharest
Ioan LIŢĂ, POLITEHNICA of Bucharest, University Center of Piteşti
Dan LASCU, Politehnica University of Timişoara
Marcel MANOFU, Continental Automotive Timişoara
Dan MANOLESCU, Association for Promoting Electronics Technology
Bogdan MIHĂILESCU, POLITEHNICA of Bucharest; APTE
Cătălin NEGREA, Darknote Engineering
Viorel NICOLAU, Dunărea de Jos University of Galaţi
Cristina OPREA, Tensor srl

Gheorghe PANĂ, Transilvania University of Braşov
Mihaela PANTAZICĂ, POLITEHNICA of Bucharest
Daniela TĂRNICERIU, Gh. Asachi Technical University of Iaşi
Adrian TULBURE, 1 Decembrie 1918 University of Alba Iulia
Liviu VIMAN, Technical University of Cluj-Napoca
Gabriel VLĂDUŢ, Romanian Association for Technological Transfer and Innovation
Maria VINȚAN, Lucian Blaga University of Sibiu

**International Advisory Body:**
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Detlef BONFERT, Fraunhofer EMFT, Munich Germany
Joseph FJELSTAD, CEO of Verdant Electronics, USA
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Pavel MACH, Czech Technical University in Prague, Czech Republic
Alain MICHEL, ANSYS France
Jim MORRIS, Portland State University, Oregon USA
Andy SHAUGHNESSY, The PCB Design Magazine and PCBDesign007, USA
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Heinz WOHLRABE, TU Dresden, Germany
Klaus-Jürgen WOLTER, TU Dresden, Germany

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**Chair**:
Cătălina NEGHINĂ, Lucian Blaga University of Sibiu
**Members:**
Cristina LEPĂDATU, POLITEHNICA of Bucharest, Association for Promoting Electronics Technology
Bogdan MIHĂILESCU, POLITEHNICA of Bucharest, Association for Promoting Electronics Technology
Rodica NEGROIU, POLITEHNICA of Bucharest
Tamara SAUCIUC, POLITEHNICA Bucharest
Elena Mirela STETCO, Technical University of Cluj-Napoca

**Exposition Committee**
**Chair:**
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**Co-Chairs:**
Adelina-Ioana ILIEȘ, Technical University of Cluj Napoca, Romania
**Members:**
Cristina Mihaela LEPĂDATU, POLITEHNICA of Bucharest, Association for Promoting Electronics Technology, Romania

**IEEE EPS Student Chapters Support Committee**
**Chair**:
Mădălin MOISE, IEEE-EPS, POLITEHNICA of Bucharest
**Co-Chair:**
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**Members:**
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Elisei ILIEȘ, Politehnica University of Timişoara
Mihai NEGHINĂ, Lucian Blaga University of Sibiu
Rodica NEGROIU, IEEE-NTC, POLITEHNICA of Bucharest
Cosmin ONCIOIU, POLITEHNICA of Bucharest
Corina SĂNDULESCU, POLITEHNICA of Bucharest
Elena STETCO, Technical University of Cluj-Napoca

**Local Committee**
**Chair:**
Cătălin CIOBANU, Transilvania University of Brașov
**Co-Chair:**
Titus BĂLAN, Transilvania University of Brașov
Vlad POPESCU, Transilvania University of Brașov
**Members:**
Corina Ioana BOGDAN, Transilvania University of Brașov
Marius CARP, Transilvania University of Brașov
Csaba Zoltán KERTÉSZ, Transilvania University of Brașov
Traian TULBURE, Transilvania University of Brașov

**Technical secretariat**
**Chair:**
Delia LEPĂDATU, POLITEHNICA of Bucharest, Association for Promoting Electronics Technology
**Members:**
Cristina LEPĂDATU, POLITEHNICA of Bucharest, Association for Promoting Electronics Technology
Bogdan MIHĂILESCU, POLITEHNICA of Bucharest, Association for Promoting Electronics Technology
Maria PĂTULEANU, POLITEHNICA of Bucharest, Association for Promoting Electronics Technology
Florentina STĂLINESCU, POLITEHNICA of Bucharest, Association for Promoting Electronics Technology

<table>
<tr><th colspan="4">Wednesday, April 2<br>The participants are encouraged to attend any activity in any TRACK that would interest them (except the ones marked as restricted)</th></tr>
<tr><td>Time frame</td><td colspan="2">Track 1<br>TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS<br>the 34th edition<br>Industry-Wide Student Challenges</td><td>Track 2<br>MICROELECTRONICS DAYS<br>the 1st edition<br>organized by the Working Group for Microelectronics of the STMS Comission of the Romanian Academy</td></tr>
<tr><td colspan="4">JOINT EVENTS WITH THE REGIONAL DEVELOPMENT AGENCY – CENTRU</td></tr>
<tr><td>09:00 – 14:30</td><td colspan="3">Registration & Exhibition opening - Welcome coffee<br>(1st floor hall)</td></tr>
<tr><td>10:00 – 12:00</td><td colspan="2">Workshop ADR Centru (EEN) (Amphitheater)<br>Intellectual Property and Intellectual Property Rights</td><td>WEHUB Digital<br>Chiplets and Heterogeneous Integration for Innovative Companies<br>(Amphitheater)</td></tr>
<tr><td>12:00 – 12:15</td><td colspan="3">Coffee Break<br>(1st floor hall)</td></tr>
<tr><td>12:15 – 14:00</td><td colspan="2">Workshop ADR Centru (EEN) (Amphitheater)<br>Integration of regional organizations into European initiatives and partnerships in the field of electronics/microelectronics</td><td>WEHUB Digital<br>Chiplets and Heterogeneous Integration for Innovative Companies<br>(Amphitheater)</td></tr>
<tr><td>13:00 – 14:00</td><td colspan="2">TIE<sub>EPLUS</sub> Final Stage (public event)<br>(Amphitheater)</td><td>Workshops or ad-hoc meetings between direct and indirect participants in IPCEI or other collaborative projects<br>(UI2, UI3, UI6 Rooms)</td></tr>
<tr><td>14:00 – 15:00</td><td colspan="3">Light Lunch<br>(1st floor hall)</td></tr>
<tr><td>15:00 – 18:00</td><td>TIE<sub>EPLUS</sub> Final Stage (public event)<br>(Amphitheater)</td><td>Technical meetings<br>(UI7 Room)</td><td rowspan="3">Workshops or ad-hoc meetings between direct and indirect participants in IPCEI or other collaborative projects<br>(UI2, UI3, UI6 Rooms)</td></tr>
<tr><td>18:00 – 18:30</td><td>Coffee Break<br>(1st floor hall)</td><td>Steering Committee Meeting (RESTRICTED to Committee members)<br>(UI7 Room)</td></tr>
<tr><td>18:30 – 19:00</td><td colspan="2">TIE<sub>EPLUS</sub> Demystifying the resolution of the proposed topics<br>(Amphitheater)</td></tr>
<tr><td>19:00</td><td colspan="3">Welcome cocktail and expo networking (1st floor hall)</td></tr>
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<tr><th colspan="4">Thursday, April 3<br>The participants are encouraged to attend any activity in any TRACK that would interest them (except the ones marked as restricted)</th></tr>
<tr><th>Time frame</th><th colspan="2">Track 1<br>TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS<br>the 34th edition<br>Industry-Wide Student Challenges</th><th>Track 2<br>MICROELECTRONICS DAYS<br>the 1st edition<br>organized by the Working Group for Microelectronics of the STMS Commission of the Romanian Academy</th></tr>
<tr><td colspan="4">JOINT EVENTS WITH THE REGIONAL DEVELOPMENT AGENCY – CENTRU</td></tr>
<tr><td>08:00 – 14:00</td><td colspan="3">Registration - Welcome coffee<br>(1st floor hall)</td></tr>
<tr><td>08:30 – 09:00</td><td rowspan="3">TIE<sub>MPLUS</sub> Final Stage (public event)<br>(UI2 Room)</td><td rowspan="3">TIE<sub>TPLUS</sub> Final Stage (public event)<br>(UI3 Room)</td><td>Welcome speech – The Romanian Academy<br>The Position of the Romanian Academy "The National Ecosystem of Micro and Nano Electronics"<br>(Amphitheater)<br>Prof. Gheorghe ȘTEFAN – Corresponding Member of the Romanian Academy, President of the STMS Commission of the Academy<br>Welcome speech – Transilvania University of Brașov<br>Prof. Ioan Vasile ABRUDAN, Rector<br>Welcome speech – Regional Development Agency ADR Centru<br>Simion CREȚU – General Manager</td></tr>
<tr><td>09:00 – 09:15</td><td>Introduction to the Agenda of the day<br>Moderator: Prof. Adrian IONESCU – STMS Commission, Romanian Academy</td></tr>
<tr><td>09:15 – 10:00</td><td>EU strategies reflected in EU and national programs (Amphitheater)<br>Round table:<br>Prof. Tudor PRISECARU, President of the Senate of the POLITEHNICA Bucharest<br>Prof. Carmen BUZEA, Vice-Rector of the Transilvania University of Brașov<br>Prof. Titus BĂLAN, Dean of the Faculty of Electrical Engineering and Computer Science, Transilvania University of Brașov<br>Dr. Andreas WILD, STMS Comission,</td></tr>
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<tr><td></td><td colspan="2"></td><td>Romanian Academy<br>Dr. Paul Andrei PĂUN, “Mihai Drăgănescu” Research Institute for AI<br>Moderators: Dr. Christian von ALBRICHSFELD, Former Country Head of Continental Romania and R&D Head</td></tr>
<tr><td>10:00 – 10:15</td><td colspan="2" rowspan="2"></td><td rowspan="2">10:00 – 10:30 - Coffee Break<br>(1st floor hall)</td></tr>
<tr><td>10:15 – 10:30</td></tr>
<tr><td>10:30 – 11:45</td><td rowspan="2">TIE<sub>MPLUS</sub> Final Stage (public event)<br>(UI2 Room)</td><td rowspan="2">TIE<sub>TPLUS</sub> Final Stage (public event)<br>(UI3 Room)</td><td>The National Platform of Semiconductor Technologies, PNTS (Amphitheater)<br>Dr. Andrei AVRAM – Technical Director IMT<br>IPCEI, the actual status in Romania<br>• The progress reached by the direct participants Speakers: representatives of Bosch, NXP, Continental<br>• The status of the indirect participants<br>Speakers: representatives of project coordinators in universities, research institutes and small and medium enterprises</td></tr>
<tr><td>11:45 – 12:15</td><td>A national ecosystem in micro and nanoelectronics (1) (Amphitheater)<br>Keynote: the contest ”Tudor Tănăsescu”, a complementary mean for the development of highly qualified specialists<br>Prof. Gheorghe BREZEANU – Politehnica of Bucharest</td></tr>
<tr><td>12:15 – 13:15</td><td colspan="3">Lunch<br>(1st floor hall)</td></tr>
<tr><td>13:15 – 15:00</td><td colspan="2">TIEμ Final Stage (public event)<br>(UI6 Room)</td><td>Complementary actions for Chips-JU (Amphitheater)<br>• Pilot lines<br>Prof. Marius ENĂCHESCU – Politehnica Bucharest<br>• Competence centers, involvement of Romania<br>Carmen MOLDOVAN – IMT<br>Financing the development of research and innovation activities</td></tr>
</table>

<table>
<tr><td></td><td colspan="3"></td><td>carried out by the business environment by using European funds during 2021-2027 – ADR Centru<br>• Contribution of RDA/RP Center 2021-2027 to the STEP Platform<br>Other EU and international initiatives<br>Prof. Adrian IONESCU – STMS Commission, Romanian Academy</td></tr>
<tr><td>15:00 – 15:15</td><td colspan="3">Coffee Break<br>(1st floor hall)</td><td>14:45 – 15:15 - Coffee Break<br>(1st floor hall)</td></tr>
<tr><td rowspan="3">15:15 – 17:00</td><td colspan="3">TIEμ Final Stage (public event)<br>(UI6 Room)</td><td rowspan="3">Panel: A national ecosystem in micro- and nanoelectronics (2)<br>(Amphitheater)<br>Coordination of the National Ecosystem:<br>Mihnea COSTOIU – Rector Politehnica Bucharest<br>• Coordination with other national programs and activities (such as ”Tudor Tănăsescu” contest, Technologies of Interconnections in Electronics – Industry-Wide Student Challenges, a.s.o)<br>• Establishing a formal group for contacts with the Romanian authorities with periodical meetings<br>Research and innovations in European and regional strategies to increase the SME competitiveness, with emphasis on the funding offered through the 2021-2027<br>Ioan LEVITCHI – Director of the Regional Policies Department, ADR Centru<br>Development of research and innovation in universities in Centru Region, with the support of European funds<br>Prof. Ana-Maria CAZAN, Dean of the Faculty of Psychology and Education Sciences, Transilvania University of Brașov<br>Synergies between PR Centru and</td></tr>
<tr><td colspan="3">Committee Assessment meetings (RESTRICTED to Committee members)</td></tr>
<tr><td>TIE<sub>MPLUS</sub><br>(UI2 Room)</td><td>TIE<sub>TPLUS</sub><br>(UI3 Room)</td><td>TIEμ<br>(UI7 Room)</td></tr>
<tr><td>17:00 – 17:45</td><td colspan="3">Technical Meetings<br>TIE<sub>E</sub> (UI2+UI3 Rooms)<br>TIE<sub>M</sub> (UI6 Room)</td></tr>
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| | | |
|---|---|---|
| | | **European Partnerships for Innovation**<br>Iceberg Consulting<br>**Session conclusions**<br>**Moderators:**<br>Prof. Adrian IONESCU – STMS Commission, Romanian Academy<br>Ovidia CABA – Director of the Department Regional Policies and Programs, ADR Centru |
| **17:45 – 18:45** | **Common Session:**<br>**TIEμ, $TIE_{M\ PLUS}$ si $TIE_{T\ PLUS}$ Demystifying the resolution of the proposed topics**<br>***(Amphitheater)*** | |
| **18:45 – 20:30** | **Award Ceremony**<br>**Keynote1: Victoria CUMMINGS – ECSA, EU Chips-Skill Academy**<br>**Keynote 2: Carolyn TUBILLO – Cadence, EDA solutions**<br>***(Amphitheater)*** | |
| **20:30** | ***Gala dinner***<br>***(Sergiana Center)*** | |
| **21:30** | **TIE Committee Chairs & European Chips Skills Academy representatives meeting (RESTRICTED)** *(UI7 Room)* | |

<table>
<tr><th colspan="4">Friday, April 4<br>The participants are encouraged to attend any activity in any TRACK that would interest them (except the ones marked as restricted)</th></tr>
<tr><td>Time frame</td><td colspan="2">Track 1<br>TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS<br>the 34th edition<br>Industry-Wide Student Challenges</td><td>Track 2<br>MICROELECTRONICS DAYS<br>the 1st edition<br>organized by the Working Group for Microelectronics of the STMS Comission of the Romanian Academy</td></tr>
<tr><td colspan="4">JOINT EVENTS WITH THE REGIONAL DEVELOPMENT AGENCY – CENTRU</td></tr>
<tr><td>08:00 – 08:30</td><td colspan="2">Preliminary activities<br>TIE<sub>E</sub> (UI2+UI3 Rooms) TIE<sub>M</sub> (UI6 Room)</td><td>Registration for Microelectronics Day 2 - welcome coffee<br>(1st floor hall)</td></tr>
<tr><td>08:30 – 08:40</td><td rowspan="3">TIE<sub>E</sub> Hackathon<br>(UI2+UI3 Rooms)</td><td rowspan="3">TIE<sub>M</sub> Hackathon<br>(UI6 Room)</td><td>Opening session: Wrap-up day 1<br>(Amphitheater)<br>Prof. Adrian IONESCU – STMS Comission, Romanian Academy<br>Dr. Andreas WILD – STMS Comission, Romanian Academy</td></tr>
<tr><td>08:40 – 08:50</td><td>Introduction on the Agenda of the day<br>(Amphitheater)<br>Moderator:<br>Prof. Paul SVASTA – STMS Comission, Romanian Academy<br>Prof. Ovidiu POP – STMS Comission, Romanian Academy</td></tr>
<tr><td>08:50 – 10:00</td><td>A National Ecosystem in Micro and Nano Electronics (3) (Amphitheater)<br>ADR Centru: Education and vocational training in smart specialization areas in the Center Region Program Priority 1, 2 and 6<br>Ovidia CABA – ADR Centru<br>CNDIPT – Dual education in the Center Region<br>Gabriel RADU – ADR Centru<br>Partnership for Education – Academic & Economic Environment<br>Aurelia FLOREA – MIELE Tehnica Brașov<br>Transilvania University of Brașov - Cooperation between universities and bussiness environment<br>Prof. Titus BĂLAN, Dean of the Faculty of Electrical Engineering and Computer Science, Transilvania University of Brașov</td></tr>
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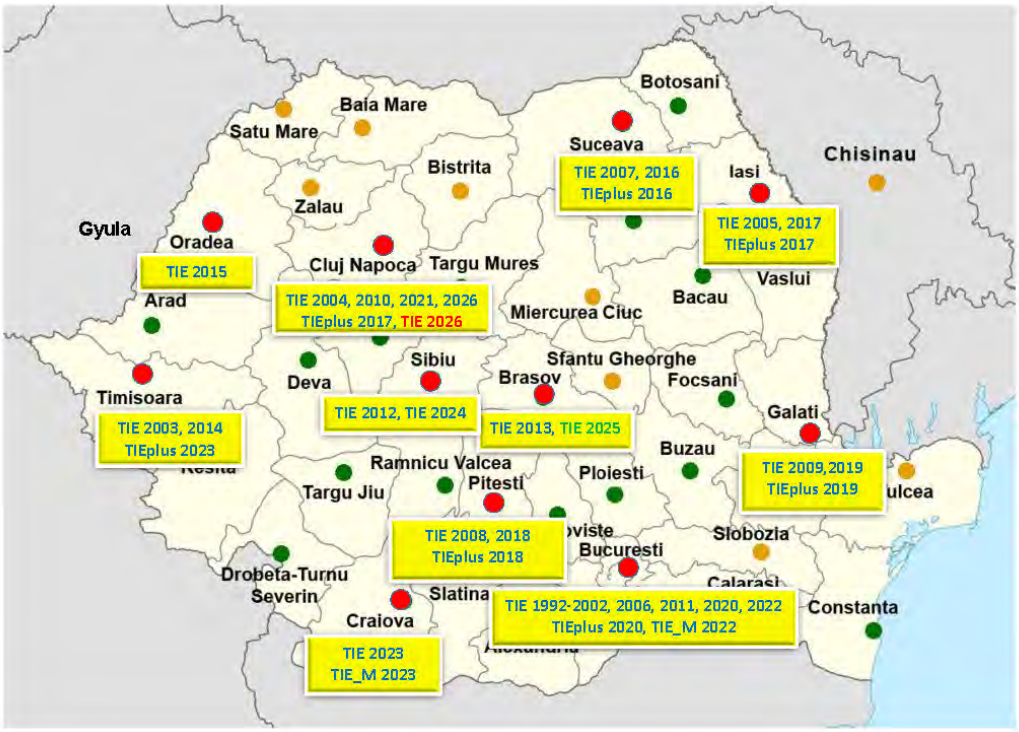
| | | | |
|---|---|---|---|
| | | | **Brașov City Hall: Regional Integrated Consortium for Dual Education Brașov, initiative to create a complete professional route for higher technical education** |
| **10:00 – 10:30** | | | ***Coffee Break, opportunity to visit $TIE_E$ & $TIE_M$ Hackathon activities*** ***(1st floor hall)*** |
| **10:30 – 12:30** | | | **TIEμ: a complementary instrument for future professional education** ***(Amphitheater)*** Assoc. Prof. Cătălin CIOBANU – Transilvania University of Brașov |
| | | | **International Panel**: **Skills Development in Electronics Packaging** ***(Amphitheater)*** Participants: Victoria CUMMINGS – ECSA, EU Chips-Skill Academy representative; Dr. Peter TRANITZ – IPC EU Silicon to Systems; Romanian delegates |
| ***12:30 – 13:30*** | ***Lunch*** ***(1st floor hall)*** | | |
| ***13:30 –14:00*** | **$TIE_E$ Assessments (public events)** ***(UI2+UI3 Rooms)*** | **$TIE_E$ Assessments (public events)** ***(UI6 Room)*** | Transfer from Transilvania University of Brașov Library to Miele Tehnica Brașov Coordinator: Aurelia FLOREA – Organizational Development & People Experience Director, Miele Tehnica Brașov |
| **14:00 – 16:30** | | | Visit at the Miele Tehnica Brașov |
| **18:30 – 19:00** | **TIE Steering Committee & Microelectronics Representatives Meeting (RESTRICTED to Committee members)** ***(UI7 Room)*** | | |
| ***19:00*** | ***Awarding $TIE_E$, $TIE_M$ & Conclusion speeches*** ***(Amphitheater)*** ***Closure Banquet*** ***(Sergiana Center)*** | | |

| **Saturday, April 5** | |
|---|---|
| **09:30 – 10:30** | **Looking Forward. Farwell discussion for the next TIE Industry-wide student challenge, TIE 2026** ***(1st floor hall)*** |

# TIE past present and future editions




| Year | University | Event |
|---|---|---|
| 1992-2002 | University Politehnica of Bucharest | TIE |
| 2003 | Politehnica University of Timişoara | TIE |
| 2004 | Technical University of Cluj-Napoca | TIE |
| 2005 | Gh. Asachi Technical University of Iaşi | TIE |
| 2006 | University Politehnica of Bucharest | TIE |
| 2007 | Ştefan cel Mare University of Suceava | TIE |
| 2008 | University of Piteşti | TIE |
| 2009 | Dunărea de Jos University of Galaţi | TIE |
| 2010 | Technical University of Cluj-Napoca | TIE |

## TIE & $TIE_M$ & $TIE_{PLUS}$ past and present editions

| | | |
|---|---|---|
| 2011 | University Politehnica of Bucharest | TIE |
| 2012 | Lucian Blaga University of Sibiu | TIE |
| 2013 | Transilvania University of Braşov | TIE |
| 2014 | Politehnica University of Timişoara | TIE |
| 2015 | University of Oradea | TIE,<br>$TIE_{Plus}$ Kick-off |
| 2016 | Ştefan cel Mare University of Suceava | TIE, $TIE_{Plus}$ |
| 2017 | Gh. Asachi Technical University of Iaşi | TIE, $TIE_{Plus}$ |
| 2018 | University of Piteşti | TIE, $TIE_{Plus}$<br>1st TIE bootcamp |
| 2019 | Dunărea de Jos University of Galaţi | TIE, $TIE_{Plus}$ |
| 2020 | University Politehnica of Bucharest - Virtual Event | TIE, $TIE_{Plus}$ |
| 2021 | Technical University of Cluj-Napoca - Virtual Event | TIE, $TIE_{Plus}$ |
| 2022 | University Politehnica of Bucharest | TIE,<br>$TIE_M$ Kick-off |
| 2023 | University of Craiova | TIE, $TIE_M$ |
| | Politehnica University of Timişoara | $TIE_{Plus}$, $TIE_M$ Plus |
| 2024 | Lucian Blaga University of Sibiu<br>Continental Automotive Sibiu | $TIE_E$, $TIE_{Plus}$, $TIE_M$,<br>$TIE_M$ Plus, $TIE_T$, $TIE_\mu$ |
| 2025 | Transilvania University of Braşov | $TIE_E$, $TIE_{Plus}$, $TIE_M$,<br>$TIE_M$ Plus, $TIE_T$, $TIE_\mu$ |
| 2026 | Technical University of Cluj-Napoca | $TIE_E$, $TIE_{Plus}$, $TIE_M$,<br>$TIE_M$ Plus, $TIE_T$, $TIE_\mu$ |

## - WORKSHOP AGENDA -
## European opportunities and initiatives to support SMEs

**Transilvania University of Brașov, Str. Iuliu Maniu, Nr. 41A**

**April 2, 2025**

**09.30-10.00** **Reception and registration of participants**

**PART I: NOTIONS OF INTELLECTUAL PROPERTY AND PROPERTY RIGHTS**

Moderator: Ms. Andreea POTINTEU, RDA Centru

**10.00-10.15** **Welcome speech:**

- Ms. Andreea POTINTEU, RDA Centru
- Assoc. Prof. Cătălin CIOBANU, Ph.D., Transilvania University of Brașov
- Prof. DHC mult. Paul Mugur SVASTA, Ph. D., Manager, Center for Technological Electronics and Interconnection Techniques, National University of Science and Technology POLITEHNICA Bucharest

**10.15-10.30** **Enterprise Europe Network - Free support services for business development: internationalization, digitalization, innovation, sustainability and resilience**

Ms. Andreea POTINTEU, Head of Business Environment Support and Investment Promotion Service – RDA Centru

**10.30-11.45** **Notions of Intellectual Property and Intellectual Property Rights**

Ms. Liliana POP, European IP Ambassador

**11.45-12.00** **Obtaining the CE marking with the support of the Enterprise Europe Network: MAX ENERGI SAVER SRL - example of good practice**

Mr. Dragoș MOTOLEA, Representative of MAX ENERGI SAVER SRL

**12.00-12.15** **Coffee break**

**PART II: INTEGRATION OF REGIONAL ORGANIZATIONS INTO EUROPEAN INITIATIVES AND PARTNERSHIPS IN THE FIELD OF ELECTRONICS/MICROELECTRONICS**

Moderator: Ms. Andreea POTINTEU, RDA Centru

**12.15-12.45** **European initiatives and partnerships in the field of electronics/ microelectronics: Chips Act and the new Alliance on Processors and Semiconductor Technologies**

Ms. Andreea POTINTEU, Head of Business Environment Support and Investment Promotion Service – RDA Centru

**12.45-13.15** **UEFISCDI**

**13.15-13.45** **Presentation of the European project ISOLDE, CHIPS JU**

Assoc. Prof. Cătălin CIOBANU, Ph.D., Transilvania University of Brașov

**13.45-14.00** **Questions and Answers Session**

*Centru Region and Regional Development Agency Centru*

# We continue our European journey and develop together the communities in the counties of Alba, Brașov, Covasna, Harghita, Mureș, and Sibiu

Centru Development Region is established based on Law 151/1998, updated by the Regional Development Law no. 315/2004, with subsequent amendments and completions, through the association of the counties of Alba, Brașov, Covasna, Harghita, Mureș, and Sibiu, in the center of Romania. The entire Region covers an area of 34,100 square kilometers, representing 14.3% of the country's territory. Due to its geographical position, Centru Region has direct connections with six of the other seven development regions, with approximately equal distances from its central area to the main border crossing points.

**The communities in Centru Region identify and define together their path to prosperity.**

Regional Development Agency Centru, a public utility NGO, is in the service of local communities and their citizens. Its actions aim to support local development and improve the living conditions of the population. The activity of RDA Centru is carried out by a team dedicated to get involved for the good of each local community. In total transparency and openness, the role of RDA Centru is to implement development plans and strategies created in partnership with the stakeholders involved in regional development from both the public and private sectors, to facilitate the efficient use of financial and human resources in order to support the communities in Centru Region. Thus, RDA Centru is a performance-oriented organization with a medium-term development vision that has contributed to setting funding priorities within the “Centru Region” Program: a region more attractive for living, investing, and working, where environmental concerns are the responsibility of every citizen.


*Împreună dezvoltăm regiunea!*

Regional development policies and European and national funds directed towards the Centru Region since Romania's accession to the European Union have significantly contributed to the transformation of the region.

Indicators that can provide an image of the current development level of the Centru Region, compared to 23 years ago, show that, at the regional level, the Gross Domestic Product per capita at purchasing power standard has increased more than five times, from approximately 5,000 euros to almost 27,000 euros in 2023. In relation to the EU27 average, this indicator has risen from 27% to 70%. Last but not least, labor productivity has increased at the regional level, from approximately 44% of the EU average in 2007, to 80% of the EU27 average in 2023, being comparable to labor productivity recorded in regions of Slovakia, Poland, Greece, Portugal, etc.

Since Romania's accession to the European Union, nearly 18,000 projects have been implemented in Centru Region through all European-funded development programs, with a total value of over 15 billion euros. The mission of RDA Centru, as an organization responsible for implementing regional development policies, is both to identify development needs within an extensive partnership framework, to formulate the Regional Development Strategy and other sectoral strategies, and to implement programs funded by the European Union's Cohesion Policy. Managing the non-reimbursable resources allocated to the Centru Region since the 2000s, RDA Centru has implemented nearly 4,000 projects, with a total value of over 3.5 billion euros. The value of the European funds absorbed through these projects exceeds 2.5 billion euros. More than two-thirds of these projects, representing over 90% of the invested funds, have been implemented after Romania's accession to the European Union.


With an experience of 26 years in the regional development process, with a long history in managing non-reimbursable European funds, starting with the pre-accession period and, after accession to the European Union, having the role of Intermediate Body for the implementation of non-reimbursable European funds, ADR Centru has - in this

programming period, 2021-2027 - the role of Managing Authority of the most important regional development program, created based on local needs and benefiting from a budget almost as large as the previous regional programs combined.

"Centru Region" Program 2021-2027 (PR Centru) aims to continue the strategic vision regarding the development of the Region, complementing the directions, actions and priorities of the Regional Development Plan (RDP 2014-2020) implemented through the Regional Operational Program 2014-2020 and through other national programs. The strategic vision of PR Centru 2021-2027, in line with the strategic vision of RDP Centru 2021-2027 and the Smart Specialization Strategy of Centru Region, is to have a cleaner region, attractive for its inhabitants and tourists, with a competitive economy based on knowledge and innovation in which care for the environment and the rational and sustainable use of resources are a priority.

Regional smart specialisation is a concept promoted by the European Commission along with the adoption of the Europe 2020 Strategy, to respond to the need to better substantiate investments, through the EU cohesion policy, in research, development and innovation. The EC recommended that national and regional authorities in Europe develop research and innovation strategies for smart specialisation, in order to make the use of structural funds more efficient, to enhance synergies between different EU, national and regional policies, as well as between public and private sector investments.

In the programming period 2014-2020, smart specialisation became an important instrument of the EU Cohesion Policy, in particular for the programming of intervention associated with the objective *"Strengthening research, technological development and innovation"* of the Common Strategic Framework. In the programming period 2021-2027,

the importance of this strategic instrument increased, being designated as an enabling condition for the Policy Objective 1 *"A Smarter Europe"*.

The development and implementation of smart specialisation strategies contributes to

increased innovation performance and economic convergence of the regions. Smart specialisation strategies support regions in transforming their needs, strengths and competitive advantages into tradable goods and services, and aim to prioritise public investment in research and innovation through a bottom-up approach aimed at the economic transformation of regions, building on regional competitive advantages and facilitating market opportunities in new interregional and European value chains. The strategies help regions to anticipate, plan and support their own economic modernisation process. The territorial approach to smart specialisation must also be supported by a factual basis, justifying interventions in terms of the sectors/areas targeted, but also determining the calibration of the assumed targets, budgets, eligible activities and regional actors involved in the intervention, taking into account the needs and absorption capacities and considering the capitalization of opportunities.

In line with RIS3, Centru Region Program 2021-2027 aims to strengthen regional RDI capacity and develop connections between the RDI environment, business and society, to create new or improved products, processes, practices, methods or services. Program support is targeted at R&D activities that exceed TRL 3. RDI activities are also aimed at research and innovation processes, technology transfer and cooperation between enterprises, RDI centres and universities with a focus on the low-carbon economy, resilience and adaptation to climate change, as well as the circular economy. Research and knowledge dissemination organisations, SMEs, and partnerships between SMEs and other types of enterprises are eligible to get financial support through grants.

Through the action "Development of RDI structures and Technology Transfer for the benefit of enterprises" PR Centru responds to the needs derived from the Program strategy and correlates sectorally with RIS3 Centru and with the demand from the regional business sector, through the alignment mechanism included in the project calls. It is supported, through projects that integrate both the investment component and the RDI activity, the building of new capacities (laboratories, testing and experimentation facilities, technological infrastructures, specific equipment including the development of different types of infrastructures that facilitate knowledge transfer such as demo-lab, living lab, fab lab, makers-space, etc. and related services) and the development, expansion and/or modernization of existing ones, being mandatory the cooperation with and the openness to the business sector. It is based on the strategic approach to regional RDI infrastructures, by including mechanisms for strategic orientation of investments, especially in relation to RIS areas, territorial distribution and avoiding overlap with the national ROADMAP.

Centru Region Program also addresses the need to support the development of connections and synergies, the creation of networks between enterprises, R&D centers and the higher education sector, the integration into innovation and knowledge networks, in relation to the regional RIS sectors/areas. The action responds to the need to integrate the regional innovation ecosystem into the European research and innovation space and to develop regional innovation networks through innovation clusters.

PR Centru also supports innovative enterprises in order to contribute to the construction of an innovative region. This action directly addresses innovation activities carried out in companies, especially SMEs, and corresponds to the challenges identified in the program strategy as well as the barriers to the diffusion of innovation according to RIS3 Centru, including through the operationalization of the Open Innovation Pilot Platform, as a pilot project to test open innovation and demand-based co-creation mechanisms (with the role of facilitator of cooperation in innovation and acceleration of market uptake of innovation) and of a venture capital fund for innovative Start-ups and Spin-offs.

*RDA Centru always remains consistent with its mission and cooperates with all those who, in any way, can and want to positively influence the path of all citizens of the Centru Region towards a better life.*

Since the Centru Region Program provides funding priorities that support the activity of research-development-innovation structures and the technology transfer towards companies, simultaneously with the industrial modernization at SME level, also establishing sustainable relations between the private and academic environment, RDA Centru supports the works of the International Conference TECHNOLOGIES AND HUMAN RESOURCES IN MICROELECTRONICS: ***TIE-2025***.

***"We must always listen to those for whom we exist and upon whom the consequences of our actions are reflected. Our activity will always be characterized by professionalism, quality and honesty, in an environment that stimulates continuous learning".***

*Simion CREȚU, General Manager of RDA Centru*

***www.regiocentru.ro*** /// ***www.adrcentru.ro***

*Împreună dezvoltăm regiunea!*

| Wednesday, April 2<br>*The participants are encouraged to attend any activity in any TRACK that would interest them*<br>*(except the ones marked as restricted)* | | |
|---|---|---|
| **Time frame** | **TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS**<br>the 34th edition<br>**Industry-Wide Student Challenges** | |
| **JOINT EVENTS WITH THE REGIONAL DEVELOPMENT AGENCY – CENTRU** | | |
| **09:00 – 14:30** | **Registration & Exhibition opening - Welcome coffee**<br>*(1st floor hall)* | |
| **13:00 – 14:00** | **TIE$_{EPLUS}$ Final Stage**<br>**(public event)**<br>*(Amphitheater)* | |
| ***14:00 – 15:00*** | ***Light Lunch***<br>*(1st floor hall)* | |
| **15:00 – 18:00** | **TIE$_{EPLUS}$ Final Stage**<br>**(public event)**<br>*(Amphitheater)* | **Technical meetings**<br>**TIE$_{MPLUS}$, TIE$_{TPLUS}$, TIE$_{\mu}$** |
| ***18:00 – 18:30*** | ***Coffee Break***<br>*(1st floor hall)* | **Steering Committee Meeting**<br>**(RESTRICTED to Committee members)**<br>*(UI7 Room)* |
| **18:30 – 19:00** | **TIE$_{EPLUS}$ Demystifying the resolution of the proposed topics**<br>*(Amphitheater)* | |
| ***19:00*** | ***Welcome cocktail and expo networking***<br>*(1st floor hall)* | |

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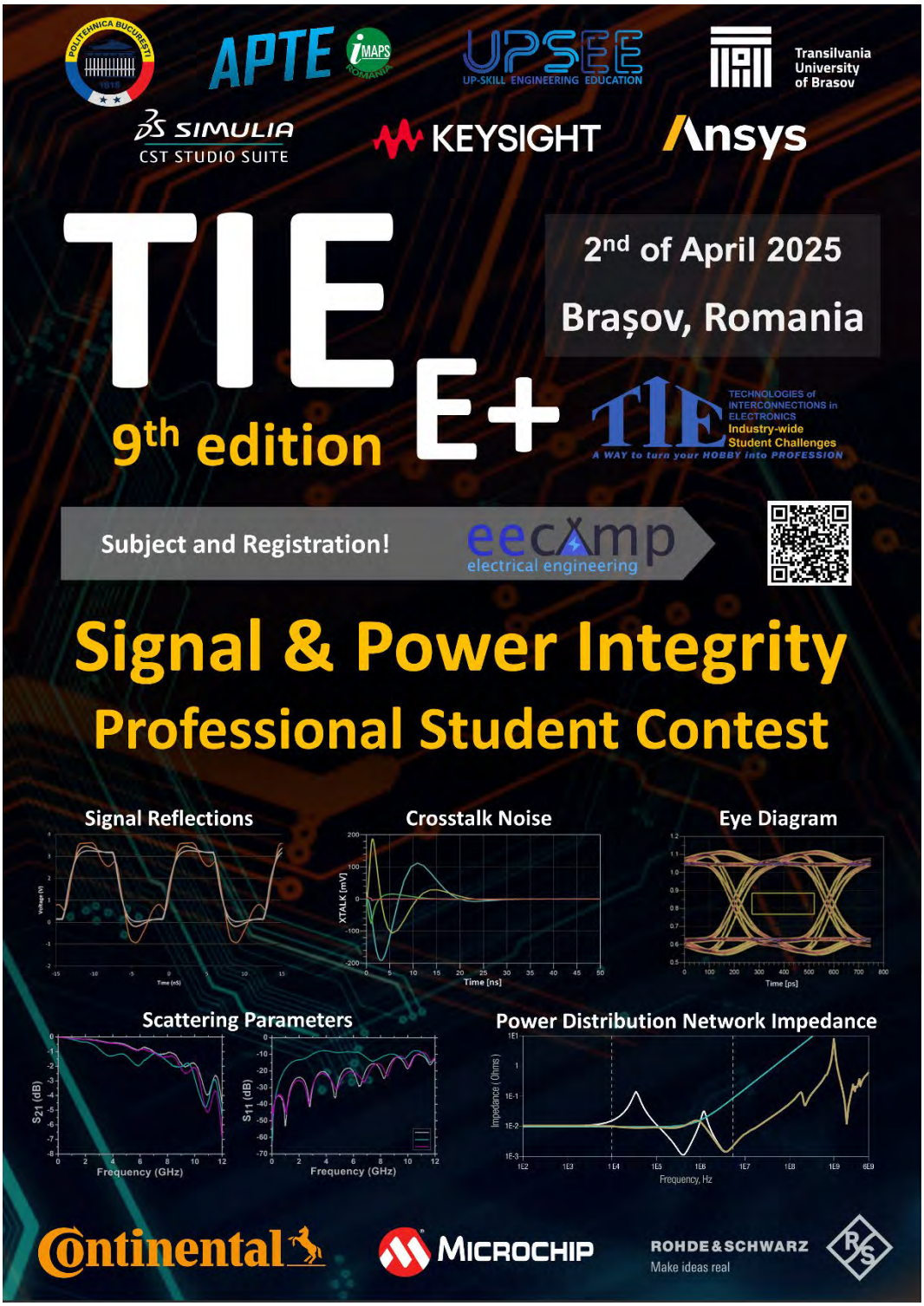
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9th edition
E+
2nd of April 2025
Brașov, Romania
TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS
Industry-wide Student Challenges
A WAY to turn your HOBBY into PROFESSION
Subject and Registration!
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Professional Student Contest
Signal Reflections
Crosstalk Noise
Eye Diagram
Scattering Parameters
Power Distribution Network Impedance
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Make ideas real

# $TIE_{EPLUS}$ – Signal and Power Integrity challenges since 2015

Launched in 2015, $TIE_{EPLUS}$ represents an evolutionary extension of the TIE brand, focusing on virtual prototyping disciplines essential for managing the complexities of high-end PCB designs. This initiative is a strategic progression aimed at fostering PCB design expertise within the Romanian electronics community. Building on the foundational knowledge acquired in the $TIE_E$ contest, which covers the intricacies of PCB layout interconnect design, $TIE_{EPLUS}$ shifts the spotlight to the critical analysis of signal and power integrity across these interconnects. Contestants are tasked with generating both pre-layout recommendations and post-layout evaluations of a given electronic module, thus demonstrating a deeper engagement with the engineering design process.

More than a competition, $TIE_{EPLUS}$ is a comprehensive educational platform that encourages students to not only assimilate new knowledge but polish highly sought-after skills. Defending their design solutions before the $TIE_{EPLUS}$ committee offers a unique opportunity for participants to enhance their analytical abilities and refine their presentation and discussion skills. This interaction underlines the multifaceted nature of PCB design, requiring a balance between performance, design constraints, and cost considerations – factoring in the technology employed in PCB fabrication and the design resources at hand.

Participating in and training for $TIE_{EPLUS}$ challenge, students are learning and developing skills needed in the industry such as:

- using and generating scattering parameters (s-parameters),
- understanding a digital interface signal timing
- properly configuring an IBIS driver and receiver to characterize or analyze a transmission channel
- defining eye-diagram and s-parameters masks
- designing PCB stack-up for high-speed signals and power-integrity
- providing pre-layout guidance for high-speed trace routing (e.g., trace dimensions, length matching strategies, via design, crosstalk analysis) and power delivery network (PDN) (e.g., DC voltage drop, AC budget analysis, decoupling capacitor strategy)
- post-layout analysis for identifying and proposing solutions to possible signal or power delivery issues in a digital interface final design
- understanding physical parameters effect over electromagnetic wave propagation
- understanding simulation parameters influence over obtained results

The TIE$_{EPLUS}$ challenge unfolds through a structured sequence of steps, designed to facilitate an engaging and educative experience for the students, while trying to emulate the typical engineering design process prevalent in the electronics industry:

- Subject Announcement – An overview of the TIE$_{EPLUS}$ theme and main topics of the subject are made available online. This gives students ample opportunity to deepen their understanding of specific digital interfaces or technologies.
- Student Enrollment – The committee conducts a thorough review of all registration submissions to ensure a level playing field. Candidates with extensive experience in SI/PI are carefully screened to maintain the competition's focus on developing talent.
- Challenge Resolution – Participants are granted a two-week period to solve the given challenge and craft their technical solutions, submitted in the form of an R&D report.
- Solution Evaluation – Following submission, contestants are expected to prepare and deliver a concise presentation (lasting 15-20 minutes) to the technical committee.

This approach not only prepares participants for the rigorous demands of the electronics design industry but also ensures that each phase of the challenge is an opportunity for learning, skill enhancement, and meaningful feedback, underscoring the competition's role as a bridge between academic learning and professional application.
The core challenge lies in effectively integrating signal integrity (SI) analysis with power distribution network (PDN) considerations. This involves ensuring that signals are transmitted with minimal distortion and interference, while also managing the power delivery to all the components in the system, to guarantee stable and reliable operation.

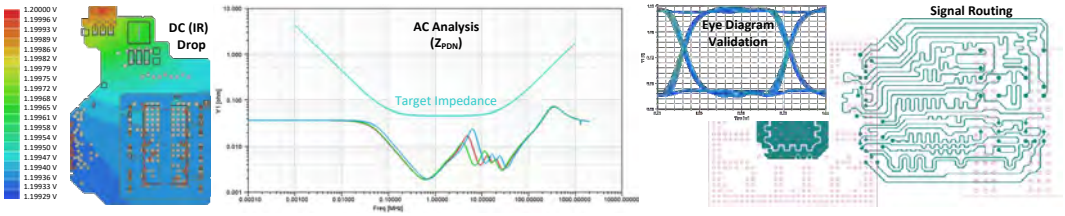


*Figure 1 Subject highlights*

In the evaluation phase of the contest, a panel comprised of experts from both the industrial sector and academic institutions comes together to meticulously review the R&D reports submitted by contestants. Prior to the oral presentations, each evaluator dedicates time to thoroughly examine the reports, formulating precise inquiries focused on the methodology and clarity of the results derived from the simulation processes.
The evaluation is structured around three core competencies:

- Software Proficiency – Examining the participant's ability to effectively employ the available simulation tools and configure the appropriate settings for accurate results.
- Theoretical Insight – Assessing the contestant's understanding of the physical principles and phenomena that are fundamental to the topics being investigated.

- Solution Excellence – Evaluating the originality, practicality, and technical soundness of the proposed solution, including how well it addresses the challenge presented.

To be recognized by the TIE$_{EPLUS}$ committee as proficient in the SI/PI domain and to be awarded a diploma, participants must demonstrate broad understanding across a wide array of topics and successfully address more than half of the subject requirements. This process ensures a rigorous standard of competence and also mirrors the professional evaluation methodologies used in industry and academia, fostering a realistic and constructive environment for learning and recognition.

**Marcel MANOFU**,
Continental Automotive Romania,
Timișoara
TIE$_{EPLUS}$ Committee Chair

**Mihai DĂRĂBAN**,
Technical University
of Cluj-Napoca
TIE$_{EPLUS}$ Committee Co-Chair

# TIE$_{EPLUS}$ Committee

**Chair:**
Marcel MANOFU, Continental Automotive, Timişoara, Romania
**Co-Chair:**
Mihai DĂRĂBAN, Technical University of Cluj-Napoca

**Technical Committee – Academic Trainers**
**Chair:**
Mihai DĂRĂBAN, Technical University of Cluj-Napoca

**Members:**
Mădălin MOISE, POLITEHNICA of Bucharest
Daniela IONESCU, Gh. Asachi Technical University of Iaşi
Gheorghe PANĂ, Transilvania University of Braşov

**Industrial Committee**
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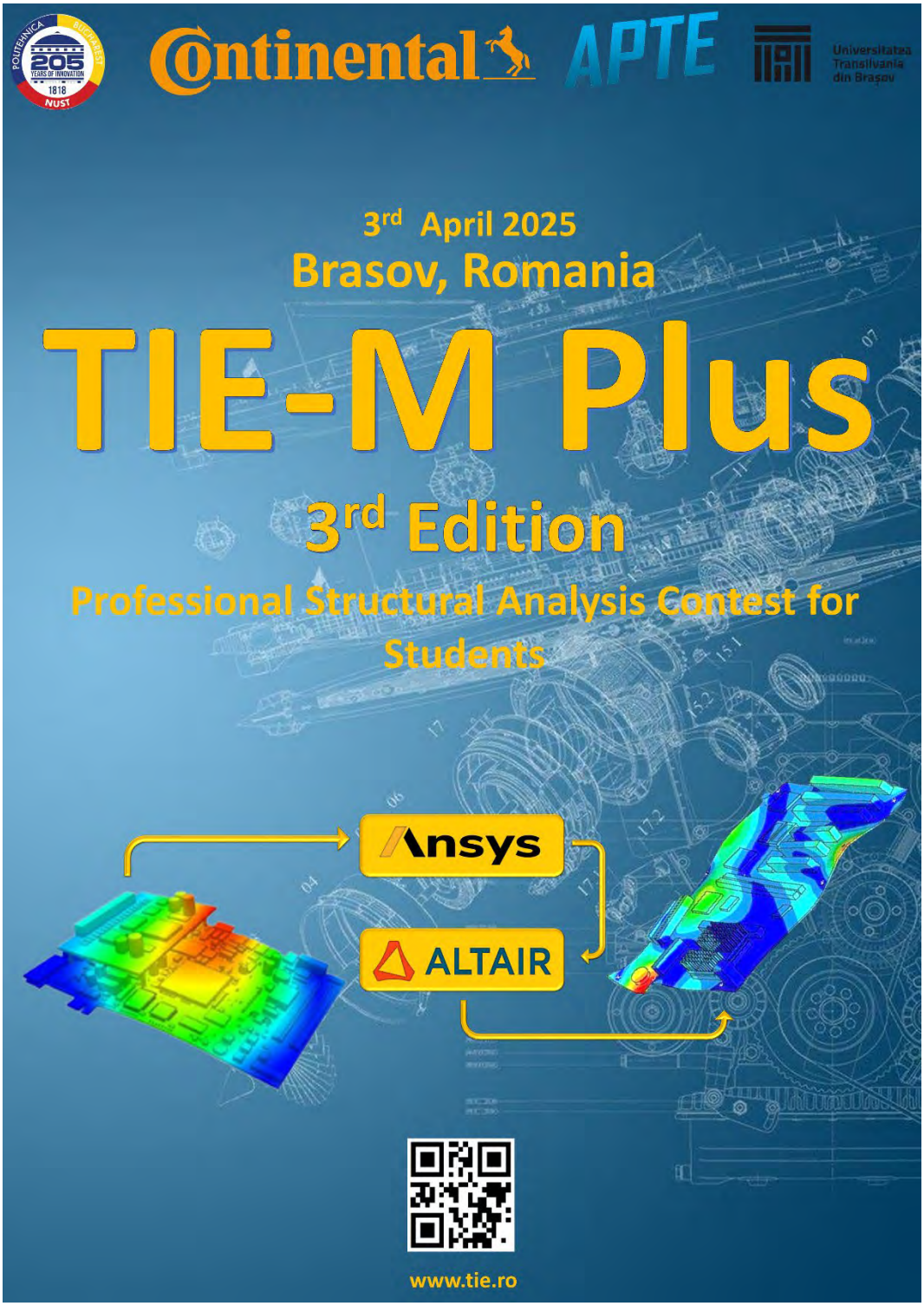
**Co-Chair:**
Radu VOINA, KEYTEK Innovation, Alba Iulia

**Members:**
Cosmin MOISĂ, Continental Automotive, Timişoara
Cătălin NEGREA, Darknote Engineering
Mihai RUS, Continental Engineering Services
Roxana VLĂDUȚĂ, Marvell Technology

| **Thursday, April 3**<br>*The participants are encouraged to attend any activity in any TRACK that would interest them*<br>*(except the ones marked as restricted)* | |
|---|---|
| **Time frame** | **TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS**<br>the 34th edition<br>**Industry-Wide Student Challenges** |
| **08:00 – 14:00** | **Registration - Welcome coffee** |
| **08:30 – 10:15** | **TIE$_{MPLUS}$ Final Stage (public event)** *(UI2 Room)*<br>**TIE$_{TPLUS}$ Final Stage (public event)** *(UI3 Room)* |
| ***10:15 – 10:30*** | ***Coffee Break*** *(1st floor hall)* |
| **10:30 – 12:15** | **TIE$_{MPLUS}$ Final Stage (public event)** *(UI2 Room)*<br>**TIE$_{TPLUS}$ Final Stage (public event)** *(UI3 Room)* |
| ***12:15 – 13:15*** | ***Lunch*** *(1st floor hall)* |
| **13:15 – 15:00** | **TIEμ Final Stage (public event)** |
| ***15:00 – 15:15*** | ***Coffee Break*** *(1st floor hall)* |
| **15:15 – 17:00** | **TIEμ Final Stage (public event)** *(UI6 Room)*<br>**Committee Assessment meetings (RESTRICTED to Committee members)**<br>**TIE$_{MPLUS}$** *(UI2 Room)* **TIE$_{TPLUS}$** *(UI3 Room)* **TIEμ** *(UI7 Room)* |
| **17:00 – 17:45** | **Technical Meetings**<br>**TIE$_{E}$** *(UI2+UI3 Rooms)* **TIE$_{M}$** *(UI6 Room)* |
| **17:45 – 18:45** | **Common Session:**<br>**TIEμ, TIE$_{M\ PLUS}$ si TIE$_{T\ PLUS}$ Demystifying the resolution of the proposed topics** *(Amphitheater)* |
| **18:45 – 20:30** | **Award Ceremony**<br>**Keynote1: Victoria CUMMINGS – ECSA, EU Chips-Skill Academy**<br>**Keynote 2: Carolyn TUBILLO – Cadence, EDA solutions**<br>*(Amphitheater)* |
| **20:30** | ***Gala dinner*** *(Sergiana Center)* |
| **21:30** | **TIE Committee Chairs & European Chips Skills Academy representatives meeting (RESTRICTED)** *(UI7 Room)* |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APTE
Universitatea Transilvania din Brașov
3rd April 2025
Brasov, Romania
TIE-M Plus
3rd Edition
Professional Structural Analysis Contest for Students
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# $TIE_{MPLUS}$: Bridging the Gap Between Industry and Higher Education

Finite element analysis (FEA) is a numerical method used for predicting how an object or an assembly behaves under given physical conditions.

Engineers in various industries heavily rely on FEA, because of its benefits including increased accuracy of prediction, better insight into critical design parameters, virtual prototyping, fewer hardware prototypes and experimental validations, a faster and less expensive design cycle, increased productivity, and, overall, an increased revenue.

Starting from 2023, TIE introduced a new section called $TIE_{MPLUS}$, focusing primarily on structural and thermal management analyses of electronic packaging. The contest provides students with a comprehensive electronic component and system development experience, concerning both its structural integrity aspects as well as its dynamic thermal behavior. Besides, this contest also helps to bring together specialists and experts from the industrial and academical partners.

Structural simulations play a crucial role in modern engineering education, providing an essential bridge between theoretical knowledge and practical application. Integrating structural simulations into university curricula equips students with the skills necessary to meet industry demands effectively. These simulations enable students to understand complex structural related behaviors (e.g., static load cases and vibrations) and explore design variations in a controlled, risk-free environment. By using state-of-the-art software and tools, students gain hands-on experience that mirrors real-world engineering challenges.

In the context of the $TIE_{MPLUS}$ competition, students were given a standardized input deck, consisting of a CAD model of an electronic module, material properties and corresponding boundary conditions. Along with the previous information the students were also given a clear roadmap towards the analyses that are needed to be performed, from which they would later extract, interpret and post-process the results.

The goal is to have the students understand the product and its weak spots, properly design a path towards its numerical evaluation (e.g., PCB deformation, natural frequency, and mode shape analysis), report their findings and give recommendations for design optimizations to improve system performance.

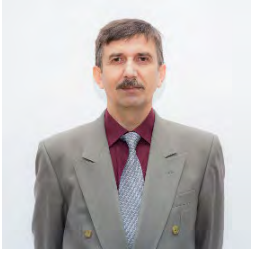
The evaluation consists of an analysis of all the submitted reports based on a thorough evaluation scale. The contestants could obtain a maximum of 100 points based on the submitted reports and in the finals, based on their presentation skills and their technical know-how to answer the questions addressed by the technical committee.

The criteria based on which the student qualifies as being initiated in the evaluated topic includes:

• Understanding the scope of the assignment
• Fundamentals of electronic packaging:
• Expertise in using FEA software to model and simulate electronic module assemblies
• Creative problem solving: innovative and efficient solutions to electronic packaging challenges
• Clear communication and reporting
• Project management: meeting deadlines, accepting feedback and handling information ethically.

This practical exposure not only enhances the students' problem-solving abilities but also familiarizes them with industry-standard practices and technologies. As a result, graduates are better prepared to transition seamlessly into professional roles, possessing the confidence and competence required to contribute immediately to the workforce. Incorporating structural simulations in educational programs thus ensures that future engineers are well-versed in contemporary methodologies, fostering innovation and maintaining the relevance of engineering education in a rapidly evolving industry landscape.

**Tamas KRAUSZ**, Continental Automotive Romania
$TIE_{MPLUS}$ Committee Chair



**Ștefan SOROHAN**, POLITEHNICA Bucharest, Romania
$TIE_{MPLUS}$ Technical Committee – Academic Trainers Chair

# TIE$_{MPLUS}$ Committees

**Chair:**
Tamas KRAUSZ, Continental Automotive Romania
**Co-Chair:**
Daniel COMEAGĂ, POLITEHNICA Bucharest

**Technical Committee – Academic Trainers**
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**Members:**
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Sergiu Valentin GALANTANU, Politehnica University of Timişoara
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Adina VATAMAN, Continental Autonomous Mobility Timișoara
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Răzvan STANCA, INAS SA

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| Atinge Fabian-Alexandru | daniel11.db27@gmail.com | Politehnica University of Timişoara |

Continental APTE Universitatea Transilvania din Brașov

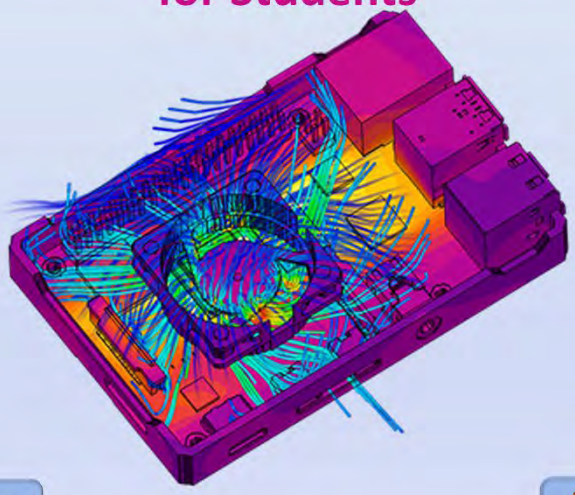
3rd April 2025

Sibiu, Romania

# TIE-T Plus

## 3rd Edition

### Professional Thermal Management Contest for Students



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# Thermal-Dynamic CAE Simulation: An Advanced Approach for Analyzing the Thermal Behavior of Technical Systems

Thermal-dynamic Computer-Aided Engineering (CAE) simulation is an advanced technique used to analyze the thermal behavior of technical systems and components under variable operating conditions. It combines thermal and dynamic analysis to provide a comprehensive view of how heat transfer and temperature fluctuations affect mechanical performance, operational efficiency, and long-term reliability of the system.

In modern engineering, thermal-dynamic CAE simulation plays a crucial role in evaluating and optimizing the performance of technical systems. By applying state-of-the-art numerical methods such as Finite Element Analysis (FEA) and Finite Volume Method (FVM), this technique allows for a detailed assessment of temperature distribution and thermal flows, as well as their impact on the materials and structures involved.

The use of FEA and FVM in thermal-dynamic CAE simulation enables detailed analysis of the thermal behavior of systems. These methods contribute to optimizing heat dissipation processes, preventing overheating, and ensuring safe and efficient operating conditions.

In the industrial sector, thermal-dynamic CAE simulation is essential for designing and validating thermal components used in fields such as automotive, aerospace, energy, and electronics. Temperature fluctuations can significantly impact the durability and performance of systems, and thermal-dynamic CAE simulations not only reduce costs associated with physical prototypes but also accelerate product development by quickly identifying problems and optimizing technical solutions.

Any system that generates or interacts with heat sources must efficiently manage heat removal to prevent overheating and performance losses. Thermal simulations are crucial in designing cooling solutions such as radiators, heat exchangers, and ventilation systems, contributing to their improved efficiency.

By using thermal simulations, thermal behavior issues can be identified and corrected during the design phase, thus reducing the need for physical tests and costly prototypes. This process leads to significant savings in time and financial resources, accelerating the product development cycle.

Many components and systems are designed to operate in extreme or variable temperature environments, such as those in the aerospace, space, or industrial sectors. Thermal simulations allow for the evaluation of the performance of these components

under conditions that would be difficult to replicate in physical experiments, thus ensuring their reliability in real operating conditions.

Now in its third edition, the TIE$_{MPLUS}$ competition aims to promote the use of CAE simulations among students from various technical faculties in Romania. Through this initiative, participants can demonstrate their skills in performing complex thermodynamic simulations by applying advanced numerical analysis methods. The competition also contributes to the development of technical skills of future engineers and familiarizes them with the software tools used in the industry to optimize the thermal behavior of technical systems.

Competitors must perform a thermodynamic simulation using CAE tools, thermally evaluating a product with four electronic components in a climate chamber environment, using natural convection and forced conduction. Based on the obtained thermal simulations, they will write a detailed report. This report will serve as the basis for analyzing and evaluating the competitors, thus determining the performance and efficiency of the proposed technical solutions.

Thermal-dynamic CAE simulation is an indispensable method in modern engineering, providing a detailed and optimized evaluation of the thermal behavior of technical systems. By applying advanced numerical methods, this technique contributes to improving the performance, efficiency, and reliability of systems, reducing costs and development time. The TIE$_{MPLUS}$ competition offers students the opportunity to directly experience these benefits, consolidating their knowledge and preparing them for future technical challenges.

**Constantin POPESCU,**
Continental Autonomous Mobility Romania
TIE$_{TPLUS}$ – Committee Chair

**Cristian-Marcel FĂRCAŞ,**
Technical University of Cluj-Napoca
TIE$_{TPLUS}$ Technical Committee –
Academic Trainers Chair

# $TIE_{TPLUS}$ - Committee

**Chair:**
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**Co-Chair:**
Philip COANDĂ, Continental Automotive Romania, Timișoara

**Technical Committee – Academic Trainers**
**Chair:**
Cristian FĂRCAŞ, Technical University of Cluj Napoca

**Members:**
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Ciprian IONESCU, Politehnica Bucharest, Romania

**Industrial Committee**
**Chair:**
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**Members:**
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Eugen DINCĂ, Continental Automotive Romania
Cristina Mihaela DRĂGAN, Continental Automotive Romania, Timișoara
Răzvan STANCA, INAS SA Craiova

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APTE
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Ansys
TIE μ
2nd edition
3rd of April 2025
Brașov, Romania
Subject and Registration!
eecamp
electrical engineering
Take on the Advanced Packaging Challenge
in Our First Chiplet-Interconnection Dedicated Contest

# TIEμ 2025 - second edition industry-wide student challenge
# Shaping the next generation of professional SiP designers

Gordon Moore famously predicted in his" Moore's Law" paper that it might become more cost-effective to construct extensive systems using smaller, individually packaged functions interconnected together. More than half a century later, the structure of the System-on-a-Chip (SoC) changes significantly with the partitioning of a monolithic die into smaller chiplets: packaging becomes one of the main focuses when designing a chip and the way the initial functionality is partitioned between multiple chiplets and how these are interconnected means we must shift our perspective to Systems in Package (SiP) (source: A. Jâjâie, A. Puşcaşu, I. Ailenei, C. B. Ciobanu and P. Svasta, "Chiplets and Next-gen Packaging Technologies in University Education," 2023 IEEE 29th International Symposium for Design and Technology in Electronic Packaging (SIITME), Craiova, Romania, 2023, pp. 207-214, https://doi.org/10.1109/SIITME59799.2023.10431355)

As the industry shifts towards heterogeneous integrations, systems in package and chiplets it becomes of paramount importance to train future engineers in these state-of-the-art techniques, including employing interposers, 2.5D, and 3D integration.

Starting in 2024, TIE introduced a new topic – TIEμ, which is addressing important subjects such as advanced packaging, 2.5D/3D integration and chiplets. In this regard, TIE is a unique approach and to our knowledge the only one of this type in Europe which bridges the gap between Universities, Industry and advanced topics such as Chiplets as shown in Figure 1. The contest brings all stakeholders to the table, ensuring industry relevant data sets are proposed as topics using state of the art EDA tools in an academic environment, in order to introduce future engineers to an upcoming future career path in advanced packaging, chiplet integration and heterogenous design.

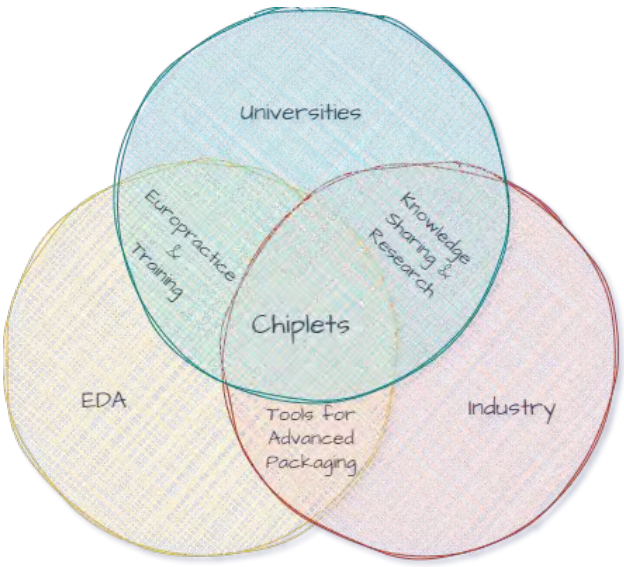



***Figure 2*** *Interaction between Industry, Universities and Chiplets*

As illustrated in Figure 2 (source: https://www.nature.com/articles/s41928-024-01126-y), the modern approach for heterogenous integration requires high speed interfaces such as Universal chiplet interconnect express (UCIe) and advanced packaging. TIEμ focuses on the new interconnection challenges for high-speed interfaces, interposers and other techniques the students need to prepare for when transitioning from SoC to SiPs. SiPs make use of specialized chiplets with customer IP and memory on the same package.

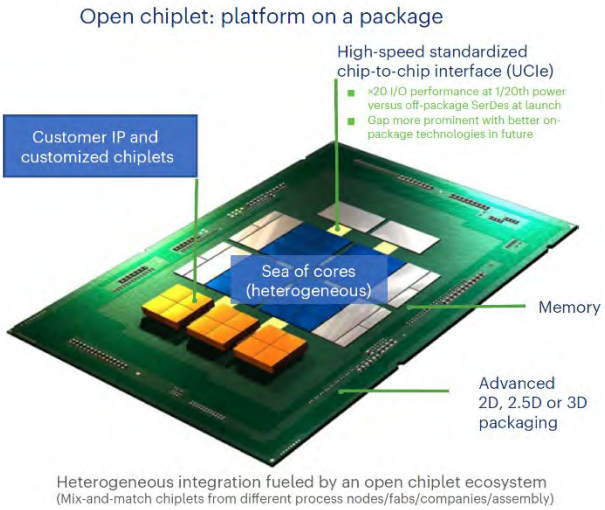
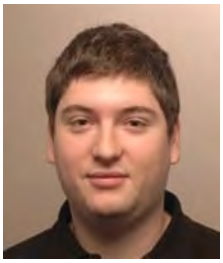



**Figure 3** Heterogeneous open chiplet on-package

The main topics necessary for designing advanced packaging and interconnects include insight in layout design (package or PCB), signal and power integrity, system in package (*SiP)* fundamentals, timing and high frequency analysis.

**Dan MANOLESCU,** APTE

TIEμ - Committee Chair



**Cătălin CIOBANU,** Transilvania University of Brașov

TIEμ - Committee Co-Chair

# TIE$_{\mu}$ - Committee

**Chair:**
Dan MANOLESCU, Association for Promoting Electronics Technology
**Co-Chair:**
Cătălin CIOBANU, Transilvania University of Braşov

**International Modelling & Simulation Environment Coordinator**
Raul FIZEȘAN, Technical University of Cluj-Napoca

**Technical support IT Department from Technical University of Cluj-Napoca**
**Chair:**
Claudiu IAKKEL, Comunication Center "PUSZTAI KALMAN ", Technical University of Cluj-Napoca

**Members:**
Cristinel Mihai MOCAN, Comunication Center "PUSZTAI KALMAN ", Technical University of Cluj-Napoca
Andraş NYAKAS, Comunication Center "PUSZTAI KALMAN ", Technical University of Cluj-Napoca

**Technical Committee – Academic Trainers**
**Chair:**
Cătălin CIOBANU, Transilvania University of Braşov
**Co-Chair:**
Raul FIZEȘAN, Technical University of Cluj-Napoca

**Members:**
Diana BRÎNARU, POLITEHNICA of Bucharest
Aurel GONTEAN, Politehnica University of Timişoara
Daniela IONESCU, Gh. Asachi Technical University of Iaşi
Csaba Zoltán KERTÉSZ, Transilvania University of Braşov
Mihaela PANTAZICĂ, POLITEHNICA of Bucharest

**Industrial Committee**
**Chair:**
Dan MANOLESCU, Association for Promoting Electronics Technology
**Co-Chair:**
Iosif ANTOCHI, NXP Romania

**Members:**
Ciprian ABRAMOV, Microchip Technology București
Dorin ANTONOVICI, IFM Sibiu
Marcel MANOFU, Continental Automotive Romania, Timișoara
Mihai SAIN, Microchip Technology București

| Thursday, April 3<br>*The participants are encouraged to attend any activity in any TRACK that would interest them (except the ones marked as restricted)* | |
|---|---|
| **Time frame** | **MICROELECTRONICS DAYS**<br>the 1st edition<br>**organized by the Working Group for Microelectronics of the STMS Comission of the Romanian Academy** |
| **JOINT EVENTS WITH THE REGIONAL DEVELOPMENT AGENCY – CENTER** | |
| **08:00 – 14:00** | **Registration - Welcome coffee**<br>***(1st floor hall)*** |
| **08:30 – 09:00** | **Welcome speech – The Romanian Academy**<br>**The Position of the Romanian Academy "The National Ecosystem of Micro and Nano Electronics"**<br>***(Amphitheater)***<br>Prof. Gheorghe ȘTEFAN – Corresponding Member of the Romanian Academy, President of the STMS Commission of the Academy<br>**Welcome speech – Transilvania University of Brașov**<br>Prof. Ioan Vasile ABRUDAN, Rector<br>**Welcome speech – Regional Development Agency ADR Centru**<br>Simion CREȚU – General Manager |
| **09:00 – 09:15** | Introduction to the Agenda of the day<br>Moderator: Prof. Adrian IONESCU – STMS Commission, Romanian Academy |
| **09:15 – 10:00** | **EU strategies reflected in EU and national programs *(Amphitheater)***<br>**Round table:**<br>Prof. Tudor PRISECARU, President of the Senate of the POLITEHNICA Bucharest<br>Prof. Carmen BUZEA, Vice-Rector of the Transilvania University of Brașov<br>Prof. Titus BĂLAN, Dean of the Faculty of Electrical Engineering and Computer Science, Transilvania University of Brașov<br>Dr. Andreas WILD, STMS Comission, Romanian Academy<br>Dr. Paul Andrei PĂUN, "Mihai Drăgănescu" Research Institute for AI<br>**Moderators:** Dr. Christian von ALBRICHSFELD, Former Country Head of Continental Romania and R&D Head |
| ***10:00 – 10:30*** | ***Coffee Break (1st floor hall)*** |
| **10:30 – 11:45** | **The National Platform of Semiconductor Technologies, PNTS *(Amphitheater)***<br>Dr. Andrei AVRAM – Technical Director IMT<br>**IPCEI, the actual status in Romania**<br>• **The progress reached by the direct participants** Speakers: representatives of Bosch, NXP, Continental<br>• **The status of the indirect participants**<br>Speakers: representatives of project coordinators in universities, research institutes and small and medium enterprises |
| **11:45 – 12:15** | **A national ecosystem in micro and nanoelectronics (1) *(Amphitheater)***<br>**Keynote: the contest "Tudor Tănăsescu", a complementary mean for the development of highly qualified specialists**<br>Prof. Gheorghe BREZEANU – Politehnica of Bucharest |
| ***12:15 – 13:15*** | ***Lunch (1st floor hall)*** |

| | |
|---|---|
| **13:15 – 15:00** | Complementary actions for Chips-JU *(Amphitheater)*<br>• Pilot lines<br>**Prof. Marius ENĂCHESCU – Politehnica Bucharest**<br>• Competence centers, involvement of Romania<br>**Carmen MOLDOVAN – IMT**<br>Financing the development of research and innovation activities carried out by the business environment by using European funds during 2021-2027 – ADR Centru<br>• Contribution of RDA/RP Center 2021-2027 to the STEP Platform<br>Other EU and international initiatives<br>**Prof. Adrian IONESCU – STMS Commission, Romanian Academy** |
| ***14:45 – 15:15*** | ***Coffee Break (1st floor hall)*** |
| **15:15 – 17:00** | **Panel: A national ecosystem in micro- and nanoelectronics (2)**<br>***(Amphitheater)***<br>**Coordination of the National Ecosystem:**<br>Mihnea COSTOIU – Rector Politehnica Bucharest<br>• Coordination with other national programs and activities (such as "Tudor Tănăsescu" contest, Technologies of Interconnections in Electronics – Industry-Wide Student Challenges, a.s.o)<br>• Establishing a formal group for contacts with the Romanian authorities with periodical meetings<br>**Research and innovations in European and regional strategies to increase the SME competitiveness, with emphasis on the funding offered through the 2021-2027**<br>Ioan LEVITCHI – Director of the Regional Policies Department, ADR Centru<br>**Development of research and innovation in universities in Centru Region, with the support of European funds**<br>Prof. Ana-Maria CAZAN, Dean of the Faculty of Psychology and Education Sciences, Transilvania University of Brașov<br>**Synergies between PR Centru and European Partnerships for Innovation** Iceberg Consulting<br>**Session conclusions**<br>**Moderators**:<br>Prof. Adrian IONESCU – STMS Commission, Romanian Academy<br>Ovidia CABA **–** Director of the Department Regional Policies and Programs, ADR Centru |
| **17:00 – 17:45** | ***Coffee Break (1st floor hall)*** |
| **17:45 – 18:45** | **Common Session:**<br>**TIEμ, $TIE_{M\ PLUS}$ si $TIE_{T\ PLUS}$ Demystifying the resolution of the proposed topics**<br>***(Amphitheater)*** |
| **18:45 – 20:15** | **Award Ceremony**<br>**Keynote1: Victoria CUMMINGS – ECSA, EU Chips-Skill Academy**<br>**Keynote 2: Carolyn TUBILLO – Cadence, EDA solutions**<br>***(Amphitheater)*** |
| **20:15** | ***Gala dinner (Sergiana Center)*** |
| **21:30** | **TIE Committee Chairs & European Chips Skills Academy representatives meeting (RESTRICTED)** |

*Name:* **Dr. Christian VON ALBRICHSFELD**
*Job position:* **Former Country Head of Continental Romania and R&D Head**
*e-mail:* **christian.albrichsfeld@continental-corporation.com**

***Short bio:***

Christian von Albrichsfeld was born in Brașov/Kronstadt (Romania) and grew up in Frankfurt, Germany. He graduated at the Technical University in Darmstadt, Germany in 1992 and received a doctoral degree in robotics and artificial intelligence from the same University in 1997. In the same year he joined the technology company Continental, being today one of the most important suppliers for the automotive industry worldwide, where he worked in research projects and in the technical management for innovative automotive systems.

From 2009 until 2025 he was the General Manager of Continental Automotive Romania, representing also as Country Head Continental in Romania, coordinating it's activities with currently more than 20.000 employees in Timişoara, Sibiu, Brașov, Nadab, Carei and Iași at national level. At the same time he is the manager for Research and Development.

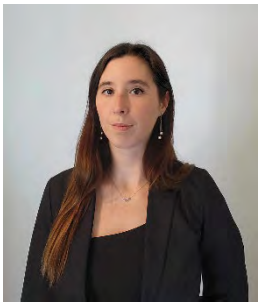
In 2012 he received the title of Honorary Professor of the Polytechnic University Timişoara. He is vice president of the German Economic Club Banat, co-president of the Executive Board of the Polytechnic University of Timişoara and vice president of the German-Romanian Chamber of Industry and Commerce. 2018 and 2022 he was awarded CEO of the Year by Automotive Today and The Diplomat.

He received the Forbes Business Award 2017 and was nominated Forbes Business Hero 2020 and Forbes Personality of the Year 2021 in the Domain Auto.

In 2023 he was awarded the title Dr. honoris causa by the Polytechnic University Timişoara.

He is permanently engaged in the collaboration between economic and educational institutions, a collaboration which not only has a scientific component, reflected in research and development but also an institutional one for improving the educational academic system and its' adaptation to global standards.

His commitment to education has also extended to the undergraduate level, being one of the initiators for reintroducing vocational schools in Romania, a project in which Continental is a partner of the pilot classes in Timişoara, Carei, Brașov and Sibiu, being also member of the German-Romanian Steering Committee for dual professional education.



***Name:*** **Victoria CUMMINGS**
***Job position:*** **Senior Manager Workforce Development & EU Projects**
***Company:*** **SEMI Europe Brussels Office**
***e-mail:*** **vcummings@semi.org**
***Presentation:*** **"Addressing semiconductor talent gap: research on industry skills needs"**

***Short bio:***
Since joining SEMI Europe in 2023, Victoria facilitates programs that support workforce development and raise awareness of the different career paths in the semiconductor sector. Currently, she acts as the coordinator of the European Chips Skills Academy (ECSA) project and is involved in several European projects related to skills development and diversity in microelectronics. Prior to entering the semiconductor industry, Victoria worked as a policy adviser for regulation on financial services and energy markets. She received a master's degree in political science from Boston University in 2018.

***Abstract:***
As the semiconductor industry continues to grow, the need for skilled professionals has become more urgent than ever. The projected 'talent gap' is expected to reach 75,000 people by 2030 meaning wide reaching, innovative solutions are needed now to expand the pool of available talent. The ECSA Skills Strategy, published in November 2024, focused on understanding and addressing the evolving skills needs in the European semiconductor sector. This study provides valuable insights into key industry questions such as:

- What emerging trends and skills will be essential for success?
- How many graduates currently possess microelectronics-relevant degrees?
- Which skills are both the hardest to find and the most sought-after in the industry?

By answering these questions, the ECSA Skills Strategy aims to provide stakeholders with data-driven insights to better align education, training, and workforce development with the industry's future needs. Whether you're a student looking to identify high-demand skills or an educator aiming to tailor curriculum offerings, this research highlights crucial pathways to success in Europe's semiconductor landscape.

***Name:*** **Carolyn TUBILLO**
***Job position:*** **Principal R&D Application Engineer**
***Company:*** **Cadence Design Systems**
***e-mail:*** **carolynt@cadence.com**
***Presentation:*** **"Introduction to Package Design and Analysis"**

***Short bio:***

Carolyn obtained her bachelor's degree in Electronics and Communications Engineering at University of Perpetual Help System Dalta in Laguna, Philippines in 2005. She has 18 years of experience in the field of substrate material qualification, IC Package Design and Electrical simulation. Started at then Philips Semiconductors but the site transitioned to NXP Semiconductors then STMicroelectronics, designing for different applications such as automotive, consumer electronics, embedded systems, etc… In 2010, she joined Nanyang Technological University (NTU) in Singapore to work on millimeter wave packages and later moved on to United Test and Assembly Centre (UTAC) in 2012, accomplishing electrical simulations and supporting package designs in all products in the company. By late 2017, she joined Socionext Europe in UK still doing package design and simulation but for network applications. Since February 2022, she has been with Cadence Design Systems working for the company's hardware products such as Palladium platform and supporting Cadence users in developing their own IC Packaging projects.

***Abstract:***

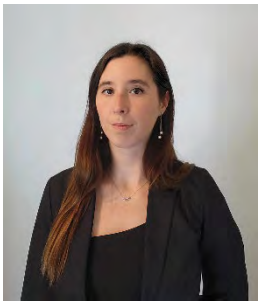
The semiconductor industry is moving from monolithic chips to the world of 3D-IC, chiplets and stacked silicon and wafer level packages. Advanced systems-on-chip (SoCs) are reaching reticle size limits, and as many companies now realize, simply following Moore's Law alone is no longer the best technical and economical path forward for the next wave of designs. As we approach the device scaling limitations at advanced nodes, the demand on compute performance and data transfer is at an all-time high. There has been a need to find innovative solutions to continue Moore's law scaling and achieve performance improvements with reduced power.

The semiconductor packaging industry is now poised to take on a larger, more significant role in electronic product design of the future. Stacking chips in the same package (3D) and a multi-chiplet system with silicon interposer on the same package (2.5D) are emerging as solutions of choice, which come with their own challenges.

To meet the market demand of the heterogenous chiplet-based architectures, new system level design methodologies are required, targeting system-level Power, Performance and Area (PPA). The Cadence Integrity 3D-IC platform is the industry's first integrated solution for system planning, implementation, and accurate early analysis. It leverages Cadence's industry-leading implementation and signoff technologies for digital, analog, and packaging through a unified hierarchical database.

| | |
|---|---|
| **Friday, April 4**<br>***The participants are encouraged to attend any activity in any TRACK that would interest them***<br>***(except the ones marked as restricted)*** | |
| **Time frame** | **MICROELECTRONICS DAYS**<br>the 1st edition<br>**organized by the Working Group for Microelectronics of the STMS Comission of the Romanian Academy** |
| **JOINT EVENTS WITH THE REGIONAL DEVELOPMENT AGENCY – CENTRU** | |
| **08:00 – 08:30** | **Registration for Microelectronics Day 2 - welcome coffee**<br>***(1st floor hall)*** |
| **08:30 – 08:40** | **Opening session: Wrap-up day 1**<br>***(Amphitheater)***<br>Prof. Adrian IONESCU – STMS Comission, Romanian Academy<br>Dr. Andreas WILD – STMS Comission, Romanian Academy |
| **08:40 – 08:50** | **Introduction on the Agenda of the day *(Amphitheater)***<br>**Moderator:**<br>Prof. Paul SVASTA – STMS Comission, Romanian Academy<br>Prof. Ovidiu POP – STMS Comission, Romanian Academy |
| **08:50 – 10:00** | **A National Ecosystem in Micro and Nano Electronics (3) *(Amphitheater)***<br>**ADR Centru: Education and vocational training in smart specialization areas in the Center Region Program Priority 1, 2 and 6**<br>Ovidia CABA – ADR Centru<br>**CNDIPT – Dual education in the Center Region**<br>Gabriel RADU – ADR Centru<br>**Partnership for Education – Academic & Economic Environment**<br>Aurelia FLOREA – MIELE Tehnica Brașov<br>**Transilvania University of Brașov - Cooperation between universities and bussiness environment**<br>Prof. Titus BĂLAN, Dean of the Faculty of Electrical Engineering and Computer Science, Transilvania University of Brașov<br>**Brașov City Hall: Regional Integrated Consortium for Dual Education Brașov, initiative to create a complete professional route for higher technical education** |
| **10:00 – 10:30** | ***Coffee Break, opportunity to visit $TIE_E$ & $TIE_M$ Hackathon activities***<br>***(1st floor hall)*** |

| | |
|---|---|
| **10:30 – 12:30** | **TIEμ: a complementary instrument for future professional education**<br>***(Amphitheater)***<br>Assoc. Prof. Cătălin CIOBANU – Transilvania University of Brașov |
| | **International Panel**:<br>**Skills Development in Electronics Packaging**<br>***(Amphitheater)***<br>Participants: Victoria CUMMINGS – ECSA, EU Chips-Skill Academy representative; Dr. Peter TRANITZ – IPC EU Silicon to Systems; Romanian delegates |
| ***12:30 – 13:30*** | ***Lunch***<br>***(1st floor hall)*** |
| ***13:30 –14:00*** | Transfer from Transilvania University of Brașov Library to Miele Tehnica Brașov<br>Coordinator: Aurelia FLOREA – Organizational Development & People Experience Director, Miele Tehnica Brașov |
| **14:00 – 16:30** | Visit at the Miele Tehnica Brașov |
| ***19:00*** | ***Awarding $TIE_E$, $TIE_M$ & Conclusion speeches***<br>***(Amphitheater)***<br>***Closure Banquet***<br>***(Sergiana Center)*** |



***Name:*** **Victoria CUMMINGS**
***Job position:*** **Senior Manager Workforce Development & EU Projects**
***Company:*** **SEMI Europe Brussels Office**
***e-mail:*** **vcummings@semi.org**
***Presentation:*** **"European Chips Skills Academy"**

***Short bio:***
Since joining SEMI Europe in 2023, Victoria facilitates programs that support workforce development and raise awareness of the different career paths in the semiconductor sector. Currently, she acts as the coordinator of the European Chips Skills Academy (ECSA) project and is involved in several European projects related to skills development and diversity in microelectronics. Prior to entering the semiconductor industry, Victoria worked as a policy adviser for regulation on financial services and energy markets. She received a master's degree in political science from Boston University in 2018.

***Abstract:***
The European Chips Skills Academy is a new initiative dedicated to advancing skills and knowledge in the rapidly evolving microelectronics sector. Bringing together 18 partners from research, industry and education across Europe, this collaborative project is committed to developing comprehensive training content tailored to meet the most in-demand skills in the semiconductor industry.
By developing targeted educational resources for new and emerging skills such as AI and machine learning, ECSA helps to build on university and vocational education to equip students and professionals with the expertise necessary to thrive in this dynamic field. A cornerstone of the project is the Student Ambassador Program, which connects motivated students with industry leaders, fostering mentorship and enhancing engagement with semiconductor related technologies. Additionally, ECSA partners with AENEAS, EPoSS, and INSIDE to host the ECS Summer School, designed to give hands-on learning experiences and invaluable insights into the semiconductor sector.
In this session you'll learn about the European Chips Skills Academy: what are the main challenges this project seeks to address and what are our objectives. You'll also hear about the different opportunities for students, including the ECS Summer School, tours of companies, and mentorship pathways to ease the jump from study to career.

***Name:*** **Dr. Peter TRANITZ**
***Job position:*** **Senior Director Technology Solutions , IPC**
***Company:*** **IPC Electronics Europe GmbH in Munich**
***e-mail:*** **Hans-PeterTranitz@ipc.org**
***Presentation:*** **"Silicon-to-Systems: Path towards Next Generation Design"**

***Short bio:***

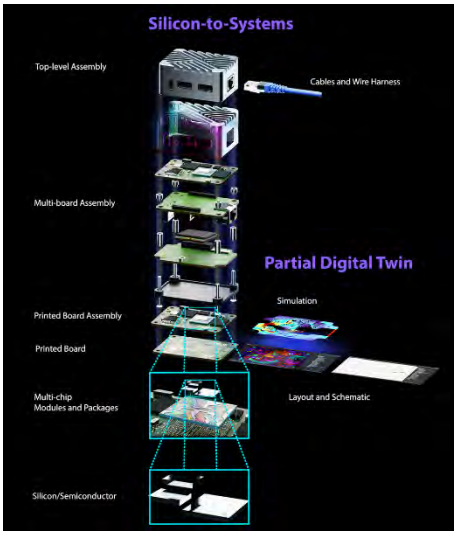
In October 2022, Peter joined the newly installed IPC Electronics Europe GmbH in Munich as Senior Director for Technology Solutions.

Peter is leading IPC's Design initiative. In this role, he is coordinating internal and external global electronic designer teams and drives the thought leadership for Design for Excellence. In addition, he supports European topics of IPC's Advanced Electronic Packaging initiative, including representing technical advocacy of the Silicon-to-Systems electronic Ecosystem on European level.

Peter is a PhD in Physics. His academic background is the creation and optical and electronic characterization of semiconductor nanostructures. The 18 years before joining IPC, Peter worked at Continental Automotive as Principal Expert and department head for the development and standardization of electro-mechanical manufacturing technologies. During this time, he led numerous global teams of experts and developed state-of-the-art electronics back-end and test technologies for the automotive industry.

***Abstract:***

IPC's Advanced Electronic Packaging strategy spans Component Level Packaging CLP and System Level Packaging SLP. Special attention requires the CLP-SLP interface that is becoming ever more important and challenging for the industry with heterogeneous integration e. g. of chiplets. Silicon to system co-design and co-optimization requires the application of multi-physics simulations.




Everything starts with Design. Therefore, the IPC Design initiative is an incremental part of the Advanced Electronics Packaging strategy. This includes the expansion of the traditional IPC offerings and development of the Next Generation Design Needs. Initiatives include Standards, Training and Certification, Events, as well as Thought Leadership.

| Friday, April 4<br>*The participants are encouraged to attend any activity in any TRACK that would interest them*<br>*(except the ones marked as restricted)* | | |
|---|---|---|
| **Time frame** | **Track 1**<br>**TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS**<br>**the 34th edition**<br>**Industry-Wide Student Challenges** | |
| **JOINT EVENTS WITH THE REGIONAL DEVELOPMENT AGENCY – CENTRU** | | |
| **08:00 – 08:30** | **Preliminary activities**<br>**TIE$_E$**<br>***(UI2+UI3 Rooms)*** | **TIE$_M$**<br>***(UI6 Room)*** |
| **08:30 – 12:30** | **TIE$_E$ Hackathon**<br>***(UI2+UI3 Rooms)*** | **TIE$_M$ Hackathon**<br>***(UI6 Room)*** |
| ***12:30 – 13:30*** | ***Lunch***<br>***(1st floor hall)*** | |
| ***13:30* – 18:30** | **TIE$_E$ Assessments**<br>**(public events)**<br>***(UI2+UI3 Rooms)*** | **TIE$_E$ Assessments**<br>**(public events)**<br>***(UI6 Room)*** |
| **18:30 – 19:00** | **TIE Steering Committee & Microelectronics Representatives Meeting**<br>**(RESTRICTED to Committee members)**<br>***(UI7 Room)*** | |
| ***19:00*** | ***Awarding TIE$_E$, TIE$_M$ & Conclusion speeches (Amphitheater)***<br>***Closure Banquet (Sergiana Center)*** | |

| Saturday, April 5 | |
|---|---|
| **09:30 – 10:30** | **Looking Forward.**<br>**Farwell discussion for the next TIE Industry-wide student challenge, TIE 2026** |


TIE
TIE E
34th Edition
University Professional
Electronics Packaging
CAD Contest for Students
April 4, 2025
Brașov, Romania
POLITEHNICA BUCUREȘTI
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APTE
AGENȚIA pentru
DEZVOLTARE
REGIONALĂ
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of Brasov
A WAY to turn your HOBBY into a PROFESSION

# TIE$_E$, migration in to Industry-Wide student challanges

In the Romanian electronics field, one of the main results of the partnership between academia and industry is the TIE$_E$ Professional Student Contest. This partnership result aims to challenge the students, year after year, to develop their abilities in CAD techniques for development of printed circuits (PCB) and electronic modules. The entire process, from designing a component with symbol and footprint, to an entire PCB with a lot of constraints and design rules, followed by the necessary fabrication files, is emphasized with this contest. Best 30…40 students from Romanian universities, and not only, are welcomed every year to solve the difficult tasks developed by industry and academia. The contest's subjects are annually updated to reflect the latest technological advancements in the industry.

Distinguished experts in electronics packaging from various companies, who form the Industrial Advisor Committee – IAC [1], work closely with academia . Together, they have significantly contributed to essential components of the competition: the subject and the evaluation scale. By doing so, the engineers involved in organizing the contest voluntarily aim to provide today's students with the kind of support and opportunities they received during their university years.
One of the TIE$_E$ main objectives is to grow a robust community dedicated to providing young and enthusiastic students with a platform to showcase the skills they have gained through their coursework, internships, and personal interests.
The main theoretical and engineering aspects that need to be assumed by participating students, include:

- designing symbols and footprints as well as the link between them;
- understanding datasheets and extracting the necessary information;
- PCB stack-up, electrical/non-electrical layers definition;
- mechanical constrains;
- thermal considerations;
- basic signal and power integrity concepts;
- placement strategies;
- routing strategies and styles;
- fabrication files creation (Gerber, N. C. Drill, BOM, assembly drawings) and their meaning.

An increasing number of students are participating in the TIE event, likely due to the numerous benefits it offers. Taking part in TIE allows students to showcase their projects to industry experts and potential employers, significantly enhancing their career prospects through increased visibility and valuable networking opportunities. Additionally, the top-performing students receive valuable certifications that confirm their proficiency in PCB design, a crucial skill in hardware engineering [1]. These certificates, recognized by leading tech companies, serve as a passport to excellent career opportunities.

All students participating in TIE$_E$ professional contest are selected, by their academic

trainers, from local contest phases. Before the contest, students might get some work packages from the organizers, to prepare for the contest, like symbols and footprints to be able to reach PCB layout phase much faster. The subject is composed from a schematic diagram which must be completed with CAD SW with 100% fidelity and a list of requirements, split into 3 parts, related to:

- library definition and schematic design;
- PCB technology, rule definition and placement and routing requirements, layout design;
- thermal management and manufacturing documentation.

Every year, the industrial committee aims to introduce new elements in the competition subject, in line with the latest trends from the today's industry:

- professional project library handling;
- antenna routing;
- flex-rigid stack-up;
- edge connectors;
- new requirements for SI/PI and SIP BGA fanout;
- specific design for manufacturing (DFM) requirements.

Each contestant is evaluated by a combined team formed by 2 or 3 members from the industry and academia, based on an evaluation scale, which is developed by the Technical Committee [TC] in collaboration with academic trainers, ensuring at the same time a clear, impartial and transparent ranking. TIE$_E$ and, finally, the whole TIE event and environment, is the proof of the voluntary joint efforts of academia and industry. This collaboration offers well prepared future engineers for the current industry challenges and the next generation of academic staff.

During the evaluation, the focus is on the comprehensive assessment of a PCB design's quality and accuracy. The evaluation process hinges on several critical factors, starting with the precise identification of components, pads, pins, footprints, and nets. Every element must align with contest-specific regulations, which may include requirements for differential pair configurations, PCB stack-up arrangements, and strict clearance and width specifications. In addition, the accurate placement of key components, such as decoupling capacitors, is essential for maintaining electrical performance. Proper routing of interconnections must respect Design for Manufacturability (DFM) and Signal Integrity (SI) principles, ensuring optimal functionality and efficiency. Thermal management is also crucial, requiring thorough calculations to prevent overheating for components or traces. Finally, the generation of complete and detailed fabrication files plays a pivotal role in transitioning the design from concept to production. This step aims to provide a structured framework for evaluating each of these critical aspects, ensuring that the design adheres to industry standards and project requirements.

All these engineering efforts evaluated by TC & IAC [1], are ranked in an order dictated by the accumulated points by each participant. According to these points, IAC establishes certifications in accordance with the scores achieved after the evaluation of participants. There are 2 types of certifications, awarded by the chairman of TIE$_E$: Schematic designer & PCB designer

The dedication of academic institutions in developing an environment for students to explore and innovate, coupled with the constant support from industry experts who provided practical insights and cutting-edge technologies has elevated the TIE$_E$ competition to a Industry-Wide student challenge. This partnership between academia and industry has created an exceptional growth opportunity, where theoretical knowledge is seamlessly integrated with real-world applications, preparing the next generation of engineers for the challenges of the future. The commitment to excellence and mentorship has not only shaped the future careers of participants, but also advanced the field, setting a new standard for future collaborations.

[1] Mihai Cenușă; Liviu Viman et all, "Advanced Collaboration in the Romanian Electronics Field based on the TIE Professional Student Contest," 2024 IEEE 30th International Symposium for Design and Technology in Electronic Packaging (SIITME), Sibiu, Romania, 2024, pp. 487-493, doi: 10.1109/SIITME63973.2024.10814785.

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# Recognition by the industry of student competences in PCB design


## TIE 2025 Certificate of Competence

The „PCB Designer” certificate is awarded, after evaluation, by the TIE IC (Industrial Committee) to selected contestants, as recognition of their high level of knowledge in the field of EDA and CAD for development of electronic modules/assemblies. The evaluation is based on the worldwide known and accepted IPC standards. The certificate is offered under the “umbrella” of the Association for Promoting Electronics Technology (APTE).

Please see more details on www.apte.org.ro.

# TIE$_E$ Committees

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| 2022 | Ciucardel Nicolae-Marian | University of Piteşti |
| 2021 | Ioniță Alexandru | Technical University of Cluj Napoca |
| 2020 | Țurca Victor | Ştefan cel Mare University of Suceava |
| 2019 | Ghineț Dragoș | Technical University of Cluj Napoca |
| | Chiraș Ovidiu Marius | Ştefan cel Mare University of Suceava |
| 2018 | Goglea Alexandru Nicolae | University of Piteşti |
| 2017 | Cojocariu Gheorghe | Ştefan cel Mare University of Suceava |
| 2016 | Voina Radu | Technical University of Cluj Napoca |
| 2015 | Luchian Teodor | Ştefan cel Mare University of Suceava |
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TIE-M
4th Edition
Professional Mechanical CAD Contest
for Students
4th April 2025
Brașov, Romania
CATIA
creo Pro|ENGINEER
SOLIDWORKS
Inventor
www.tie.ro

# TIE$_M$ -Mechanical

**TIE$_M$ -Mechanical** is a CAD Design Challenge that aims to assess students' proficiency in computer-aided design (CAD) for mechanical components, with a focus on electronic packaging and electro-mechanical assembly as shown in Figure 1. This challenge evaluates students' knowledge and skills acquired through coursework in mechanical engineering, emphasizing the design and manufacturing of mechanical components using CAD software. The challenge seeks to establish itself as a benchmark certification in the field of mechanical CAD design, particularly within the context of electronic packaging and electro-mechanical systems.

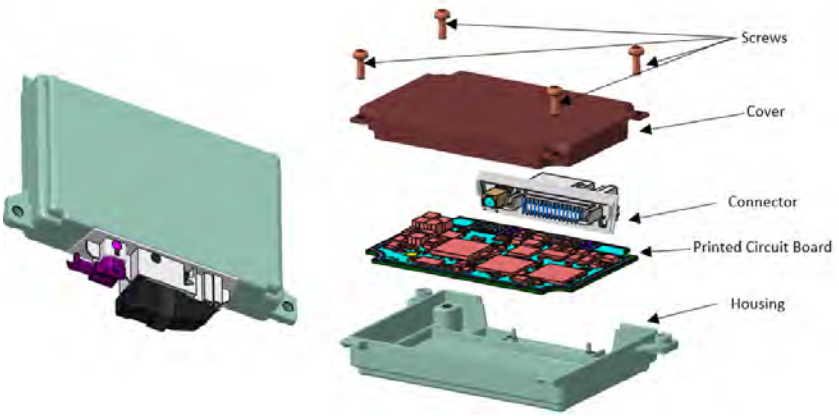



Figure 1. Electro-mechanical assembly

**Objectives:**

- Stimulating student's interest in mechanical engineering and CAD design, particularly in the context of electronic packaging and electro-mechanical assembly.
- Evaluating student's CAD design skills within a competitive framework, fostering a spirit of excellence and innovation in mechanical component design for electronic systems.
- Certifying student's CAD proficiency endorsed by industry experts, including the Industrial -Advisory Committee (IAC), to meet industry standards and requirements for electronic packaging and electro-mechanical assembly.
- Providing the electronics industry with a pool of skilled CAD designers ready to contribute to various electro-mechanical engineering projects, including electronic packaging solutions.
- Familiarizing students with the processes involved in designing mechanical components and assemblies for electronic packaging, ensuring compatibility with electronic modules and adherence to packaging standards.

- Cultivating a high level of professionalism in the use of CAD software systems for mechanical engineering applications in the context of electronic packaging and electro-mechanical assembly.
- Increasing awareness within the mechanical engineering and electronics industries about available talent and fostering strong partnerships between academia and industry in the realm of electro-mechanical engineering.
- Generating increased demand for mechanical engineers with CAD design skills specialized in electronic packaging and electro-mechanical assembly among current students and expanding job opportunities within the industrial sector.

**Description of a subject (summary)**

As a mechanical design engineer, your company won a project to create a sensor module for a well know OEM car manufacturer. To boost profits and speed up development, the company chose to use existing components (Figure 2) and make design ajustments to meet the client's needs. Modifications to the bracket and sensor ensure they fit within specified areas without altering overall functionality. The client provided a 2D drawing ("Cover.pdf") as a starting point for the cover design, which must be optimized to meet all requirements. The 3D model includes restricted areas for the new parts.

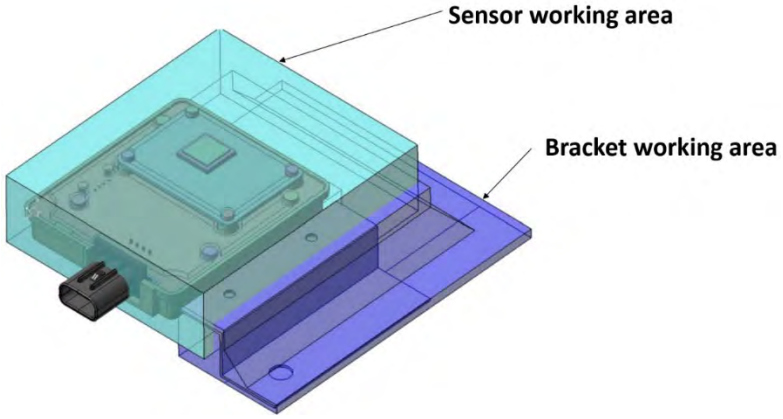
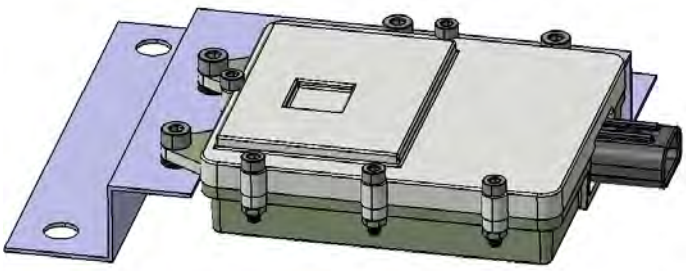



Figure 2 Existing components

**Solution**



**The criteria on the basis of which the student qualifies as being initiated in the evaluated topic:**

- Understanding Electronic Packaging: Show knowledge of how to place electronic components and manage heat within CAD designs.
- Efficient Component Integration: Ability to seamlessly integrate electronic parts into mechanical designs while meeting industry standards.
- CAD Proficiency: Expertise in using CAD software to design, model, and simulate electronic assemblies.
- Creative Problem-Solving: Demonstrate innovative solutions to electronic packaging challenges within CAD designs.
- Detail-Oriented Design: Attention to detail in CAD designs, including precision in measurements, accurate placement of components, and consideration of assembly constraints and tolerances for electronic packaging.
- Compliance with Standards: Ensure that CAD designs meet industry standards and client requirements.
- Clear Communication: Clearly convey design intentions through CAD drawings and documentation for effective collaboration.
- Professionalism: Maintain professionalism by meeting deadlines, accepting feedback, and handling information ethically.

**Alina SPÂNU**,
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## www.ulbsibiu.ro


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# Bosch Engineering Center in Cluj

Since its establishment in 2013, the Bosch Engineering Center in Cluj has played a key role in the great transformation of the mobility sector. With its extensive expertise in software, hardware & mechanical engineering and reliability engineering, as well as in sales planning, the center contributes to the development of innovative products and services based on artificial intelligence (AI) applied in the fields of automated driving, electric and connected mobility.

Whether it is advanced driver assistance systems, electric power steering systems, traditional and electric propulsion systems, various services for the automotive industry - we have extensive experience in developing innovative software and hardware solutions. We are also a leading leader in the field of artificial intelligence technology in the automotive industry with the largest team of AI specialists in Romania.

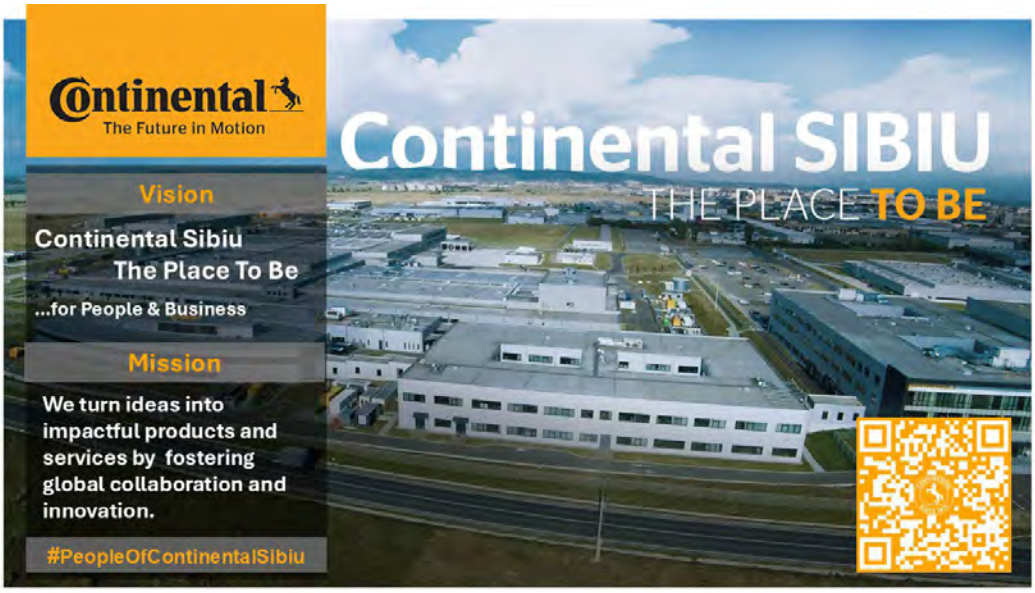
Thanks to complex technical projects, our contribution to the development of innovative Bosch products, professional and personal development opportunities for colleagues, flexible working methods, modern offices and laboratories in Cluj-Napoca and Jucu, we are one of the most sought-after employers among engineers and IT specialists in Romania.

Our promise to our colleagues is a firm one: we develop together, enjoy our work and inspire each other.

Continental develops pioneering technologies and services for sustainable and connected mobility of people and their goods. Founded in 1871, the technology company offers safe, efficient, intelligent and affordable solutions for vehicles, machines, traffic and transportation. In 2024, Continental generated preliminary sales of €39.7 billion and currently employs around 190,000 people in 55 countries and markets.
In the time frame 1999 - 2023, Continental invested over € 2,3 billion in its Romanian operations. All three group sectors of the corporation are represented in Romania. The company has five production units and four research and development centers in the cities of Timişoara, Sibiu, Carei and Iași. Continental has a tire distribution center in Bucharest. The company employed more than 20.300 colleagues by the end of 2023, out of which more than a third are engineers.

Continental Sibiu annually manufactures approximately 40 million electronic control units. The products developed, tested, and manufactured in Sibiu include intelligent braking systems, driving assist systems or connectivity systems. At present, Continental Sibiu has around 4000 employees. Together, they combine their knowledge in software and hardware development, design and simulation experience, innovation in artificial intelligence, big data, and production processes.

Discover Continental Sibiu: https://youtu.be/Synu3ls4jC0?feature=shared



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**ICCO EMT**, is a leading technical distributor of equipment and related materials to the microelectronic & advanced technology sectors, as well as electronic assembly having solution from Kulicke & Soffa, OMRON or AMX.
Our commitment is to provide our customers with first-class technology and complete services, from the configuration and the supply of the equipment, continuing with installation, programming, and maintaining the equipment, and finally, concluding with training the customer's personnel and supporting thecustomers during the product ramp-up period.
Due to the high diversity of the products we offer to our customers, we are now able to configure and provide turn-key solutions for electronic production, fully functional manufacturing lines, including ball bonding, wedge bonding, advanced dispensing solutions, sintering process, P&P equipment, electronic testing equipment, wave and reflow ovens, coating systems, electronic production automated machinery, soldering repair, rework tools.







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OMRON

# ifm – Technology, Innovation and Quality in Automation

The German group **ifm**, a global leader in the development of sensors, automation systems and digital solutions, is present in Romania (Sibiu) through three divisions:

- **ifm efector** – production of position sensors
- **ifm prover** – production of process sensors
- **ifm electronic** – sales division

Founded in 1969, **ifm** combines the strength of an international group with the flexibility of a medium-sized company, with 9,005 employees in 150 countries..

## What defines us?

✓ Open and people-oriented management
✓ Fast and efficient decision-making
✓ Investments in employee development
✓ Modern work environments
✓ Promoting a healthy lifestyle

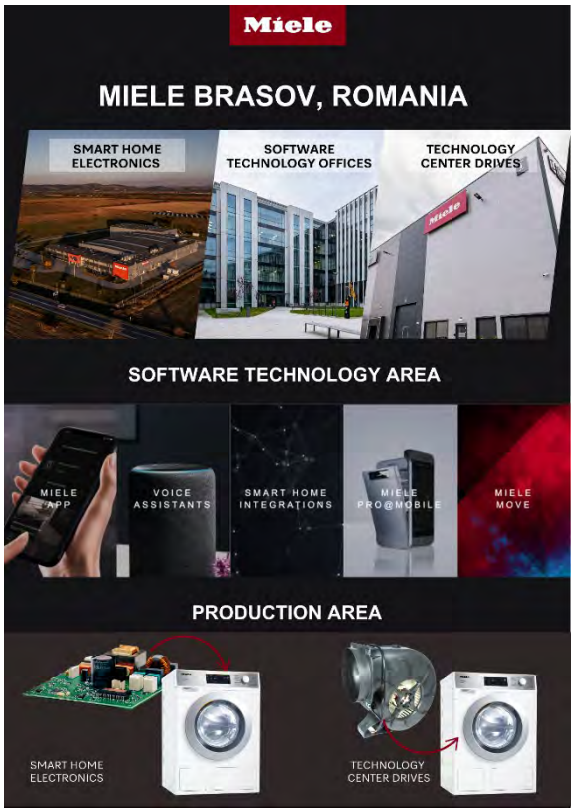
**Our mission** is to become a benchmark in the Western Industrial Zone of Sibiu, being not just a supplier, but a trusted partner for customers and an exceptional employer.

◇ **ifm values**:
✅ **Innovation** – Cutting-edge technology for automation
✅ **German quality** – Reliable, rigorously tested products
✅ **Customer orientation** – Personalized consulting
✅ **Sustainability** – Energy-efficient solutions

**ifm solutions** for industry:
📌 **Industrial sensors** – proximity, position, pressure, temperature detection
📌 **Diagnostic systems** – monitoring and predictive maintenance
📌 **Controllers & IO-Link** – efficient communication between devices
📌 **Software Industrie 4.0** – real-time data analysis

**Industries served**:
🚚 **Automotive** – Automation and quality control
🍏 **Food industry** – Production process safety
📦 **Logistics & Transport** – Smart Monitoring
⚡ **Energy & Environment** – Efficiency and Sustainability

💡 At **ifm**, we continuously innovate to contribute to a more efficient and sustainable future!




## Miele - Premium brand for 125 years

As the world's leading manufacturer of premium domestic appliances, we create delightful experiences – not only regarding the quality of our products, but also in terms of performance, design, technology, and sustainability.

**Miele** is an independent family-owned company since its establishment in 1899 and is equally committed to its owners, employees, customers, suppliers, the environment and society.

Miele stands for long-term thinking and planning, continuity of values and goals, good relationships with customers and suppliers, as well as an employee-oriented corporate and leadership culture. Miele offers products to its customers that set the standards for durability, performance, ease of use, energy efficiency, design and service.

**Since 2009, Miele Tehnica in Brașov, Romania,** has been part of this legacy , experiencing sustainable growth. Today Miele Brașov represents a reliable partner for the entire **Miele Group.**

**As part of the Smart Home Electronics division**, we have developed business areas in Brașov:

- since 2009 - Operations Electronic Production area
- since 2015 - Software Technology Development Center area
- since 2021 - Global IT Services area
- since August 2024 - Operations Technology Center Drives area

**Within the Software Technology Area**, we have been developing new competencies since 2015, growing our business with the Development Center

Area (Electronic Product Development and Digital Product Development) and the Global IT (IT Service Desk, IT Infrastructure, and IT Engineering).

We create and develop innovative digital solutions that inspire customers.

Our skilled colleagues design advanced solutions that enhance the Miele experience for users around the globe.

**At our state-of-the-art Production Plant** in Feldioara we assemble electronic power boards and mechanical components that serve as the core of the control systems for Miele appliances.

**Within the Technology Center Drives** in Brașov, we perform the pre-assembly and final assembly of the various systems that will later be installed in Miele appliances.

Our vision in Brașov "We at Miele develop ourselves to have a premium experience" is derived from Miele's philosophy "Immer Besser" /„Always Better".

Keeping this vision in mind , we ensure that we deliver a Premium Employee and Customer Experience.

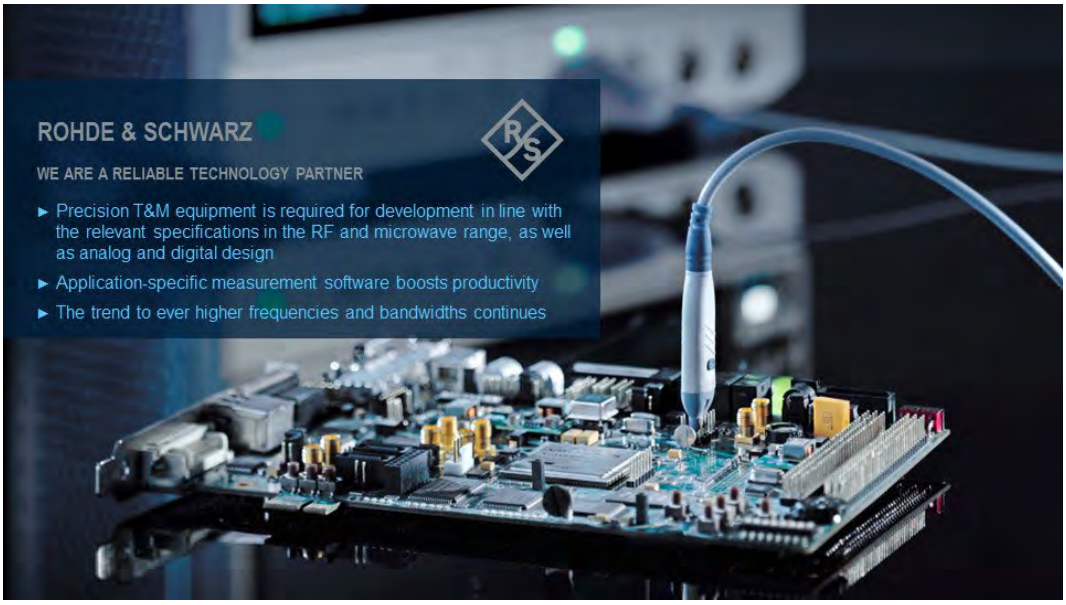
As a world leader in secure connectivity solutions for embedded applications, NXP Semiconductors is pushing boundaries in the automotive, industrial & internet of things (IoT), mobile, and communication infrastructure markets while delivering solutions that advance a more sustainable future.

The company has had substantial growth over the last few years, with currently 1100 team members at NXP Romania in Bucharest and Sibiu.

NXP Romania contributes to the development of solutions for automotive, consumer and industrial IoT markets by developing software platforms that integrate NXP components and software from partners. In addition to software development, NXP also invests in research as part of intellectual property creation programs.

Each year, NXP Romania hosts interns who learn the specifics of software development in Automotive, Edge Computing and IoT. We are proud that our interns extend their experience with practical contributions in real-life projects.

**Search for latest internship openings on:**




**Rohde & Schwarz** is a global technology group striving for a safer and connected world. With its Test & Measurement, Technology Systems and Networks & Cybersecurity Divisions, the company creates tomorrow's innovations today. The company's leading-edge products and solutions empower industrial, regulatory and military customers to attain technological and digital sovereignty.

Innovation has been part of Rohde & Schwarz since the very beginning. The company founders Dr. Lothar Rohde und Dr. Hermann Schwarz were technological pioneers. With their hands-on entrepreneurial spirit, the two college friends entered the unexplored field of RF engineering. Ninety years later, the company is still pushing technological boundaries – as a successful shaper of cutting-edge technologies such as artificial intelligence (AI), 6G, cloud and quantum technologies.

The privately owned company is known for stability and resilience. Independence is at the core of its entrepreneurial identity. The company finances its growth with its own resources. Because the company does not have to think in terms of quarterly results, it can plan sustainably for the long term. The high added value of Rohde & Schwarz makes the company a reliable, trustworthy and relevant partner for its customers.

| TEST & MEASUREMENT | TECHNOLOGY SYSTEMS | NETWORKS & CYBERSECURITY |
|---|---|---|
| Wireless I Industry, Components & Research I Aerospace & Defense Testing I Automotive | Secure Communications I Critical Infrastructure & Networks I Government I IP Network Analytics I Broadcast, Amplifiers & Media | Endpoint Security I Secure Networks I Certified & High-Grade Crypto Solutions |

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The Eberspächer Group ranks as a leading system developer and supplier in the automotive industry. The family-owned company stands for innovative solutions in exhaust technology, thermal management, and automotive electronics for different vehicle types. In classic drives and in e-mobility, Eberspächer components and systems ensure increased comfort, higher safety, and a clean environment.

The R&D center in Cluj-Napoca, Eberspaecher Controls Ro, is focused on design and development for e mobility projects, like the new generation of control units for electrical heating solutions and energy management systems for both batteries and super-capacitors.


Over the last 4 years the team in Romania reached 52 coleagues, most of which engineers in areas Basic Software and DevOps, Algorithms/Model Based Development, and Functional Testing.

**Keytek Innovation** is a design house capable of ensuring the development, security, and efficiency of custom electronic systems from idea to production, regardless of any challenges that may arise during the process. Our analytical skills and critical thinking, combined with a solid background in electronic engineering and hardware system design, will help you reduce time-to-market while keeping the development process cost-effective.

At Keytek, we boast extensive experience in High-Density Interconnect (HDI) PCB design, and we utilize cutting-edge 3D Electromagnetic (EM) analysis software and circuit simulation tools to perform signal and power integrity analysis. We understand the importance of this in today's digital world, where new standards require higher data rates, faster speeds, and increasingly complex designs. To shorten the debugging time, ensure product performance, and preemptively address future issues, our design process includes a comprehensive suite of analysis and verification techniques. Ensuring consistency, repeatability, and reproducibility are our primary objectives when validating and verifying various systems. To guarantee the success of these processes, we utilize measurement instruments from industry-leading companies and post-process the results using various programming languages specifically designed to streamline the validation and verification steps.

## Building the Future of Data Infrastructure

**Marvell Technology, Inc. (NASDAQ: MRVL)** develops and delivers semiconductor solutions that move, store, process and secure the world's data. As a trusted leader in essential data infrastructure semiconductor technology, Marvell's cloud-optimized silicon powers innovation in cloud and AI, carrier infrastructure, automotive and enterprise networking markets. With a comprehensive portfolio of electro-optic, Ethernet, processor, security and storage products and IP, the company offers merchant, semi-custom and fully custom options to address a range of customer requirements.

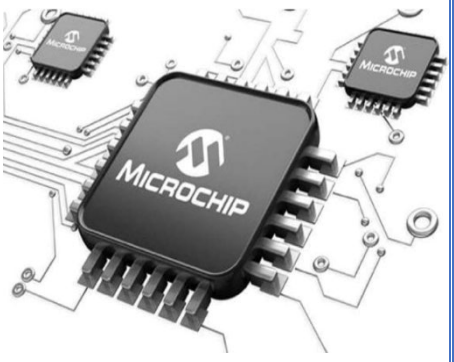
- Fabless semiconductor company
- Innovating since 1995
- 10,000+ patents worldwide
- Headquartered in Santa Clara, California
- Research and development centers located in USA, Israel, India, Vietnam, Argentina, Italy, Canada, Germany, and China
- Focused on excellence in Engineering with 85% of employees in technical roles

To learn more, please visit us at www.marvell.com.
Scan the QR code to view the Marvell 101 video.

## Microchip Technology Inc.

**Microchip Technology** is a leading provider of smart, connected and secure embedded control solutions. As a global company with over 20,000 employees, Microchip has a robust presence in Romania. Our company has an extensive portfolio that includes advanced **microcontrollers, digital signal controllers, microprocessors, mixed-signal, analog, interface, and security solutions**. Our innovative solutions empower a diverse clientele, serving customers across key sectors such as **industrial, automotive, consumer, aerospace and defense, communications, and computing**.

**Romania Design Center (RDC) – A Hub of Technological Excellence**




At the heart of our innovation lies the **Romania Design Center (RDC)** a crucible of talent and expertise accommodating over **multiple business units**. Furthermore, it is a nucleus for **software development, field technical customer support**, and the design and application development of **8-, 16-, and 32-bit microcontrollers and microprocessors**.

Strategically located in the **AFI Business Park,** adjacent to the Electronics, Telecommunications and Information Technology (ETTI), the RDC is not just a workplace but a nurturing ground for budding engineers.

**PCBflow is Siemens** first step toward PCB assembly online solutions which automate the design-to-manufacturing handoff process. With a leading position across the design-to-manufacturing flow, Siemens is the first company to offer a marketplace featuring online, fully automated DFM analysis technology, which can help optimize designs, reduce front-end engineering cycles, and streamline designer/manufacturer communication.

Powered by the industry-leading **Valor™ NPI** software engine, which performs over 1000 DFM checks, PCBflow enables PCB design teams to rapidly identify manufacturability violations. These violations are then sorted and prioritized according to level of severity, guiding users through images and locations on the design for easy identification and immediate correction.

**Siemens AG** (Berlin and Munich) is a global technology powerhouse that has stood for engineering excellence, innovation, quality, reliability and internationality for more than 175 years. Active around the world, the company focuses on intelligent infrastructure for buildings and distributed energy systems and on automation and digitalization in the process and manufacturing industries. Siemens brings together the digital and physical worlds to benefit customers and society.

**Syntegra Security SRL** is a private commercial company, established in 2008, specialized in the design, installation and maintenance of electrical installations and physical security systems (intrusion detection and alarm systems, access control systems, closed circuit television, fire detection and alarm systems).

**CERTIFICATION**

- SC Syntegra Security SRL is authorized by the General Inspectorate of the Romanian Police with license 2725/T from 4.04.2013 in order to design, install and maintain burglar alarm systems;
- SC Syntegra Security SRL holds the following authorizations from the General Inspectorate for Emergency Situations:
  - Authorization Series A no. 2404 of 03.03.2023 for the design of signalling, alarm and fire warning systems and installations;
  - Authorization Series A no. 2405 of 03.03.2023 for installation and maintenance of signaling, alarming and alerting systems and installations in case of fire;
- SC Syntegra Security SRL holds the following certificates from the National Energy Regulatory Authority:
  - Certificate no. 21486 of 22.02.2024 of type Be for "execution of external/internal electrical installations for civil and industrial premises/construction, aerial and underground connections, at the nominal voltage of 0.4 kV";

Certificate no. 21487 of 22.02.2024 of type C1A for "design of electrical lines, overhead or underground, with a nominal voltage of 0.4 kV ÷ 20 kV, transformer stations with a nominal voltage higher than 20 kV, medium voltage stations, such as and the medium-voltage electrical part of high-voltage substations".

Proiectul WE HUB for digital transformation

Co-funded by the European Union

EDIH European Digital Innovation Hubs Network

# Wallachia eHUB
# Drive innovation and digitalisation to growth

## Free services offered by Wallachia eHUB for SME companies

**SUPPORT TO FIND INVESTMENTS**

**TEST BEFORE INVEST**

**SKILLS DEVELOPMENT AND PROFESSIONAL TRAINING IN THE DIGITAL WORLD**

**CREATING DIGITAL COMMUNITIES AND NETWORKING**

Through the Wallachia e-Hub project, we increase the digital capacity of SMEs and LPAs, in order to develop processes, products, digital services and interoperability, by offering specialized services based on advanced technologies such as AI, cyber security, robotics, mobility, location technologies (GIS), Building Information Modeling (BIM), etc.

With a total value of 3,172,262.50 euros, the Wallachia e-Hub project is financed by the Digital Europe Program (EC/101083410) - WeH and by the Increasing Intelligence, Digitization and Financial Instruments Program (POCIDIF/1147/2/1/161799), being implemented between January 1, 2023 and December 31, 2025.

Project Coordinator:

**Contact details:**
Bogdan MIHĂILESCU – bogdan.mihailescu@apte.org.ro

If you fulfil the eligibility conditions please apply here:

TRiREME
DIGITAL & GREEN SKILLS TOWARDS FUTURE OF THE MOBILITY ECOSYSTEM

Co-funded by the European Union

## TRIREME Project

DigiTal & GReen SkIlls TowaRds FuturE of the Mobility Ecosystem

**TRIREME** is a 4 year Erasmus+ funded project aimed at developing tools and activities to enhace skills and foster collaboration within the automotive sector, facilitating the transition towards a greener and more digital future. The project aligns with the European Pact for Skills and its respective large-scale Partnership, the Automotive Skills Alliance.

4-year **ERASMUS+ Blueprint** Project (2024 – 2028)

31 project partners from the **Automotive Skills Alliance** partnership


**Support skills agenda in the Automotive-Mobility Ecosystem through the Large-scale Pact for Skills Partnership**

AUTOMOTIVE SKILLS ALLIANCE

**Contact details:**
Bogdan MIHĂILESCU – bogdan.mihailescu@apte.org.ro

APTE

## **ELINCLUS** ELectronic INnovation CLUSter

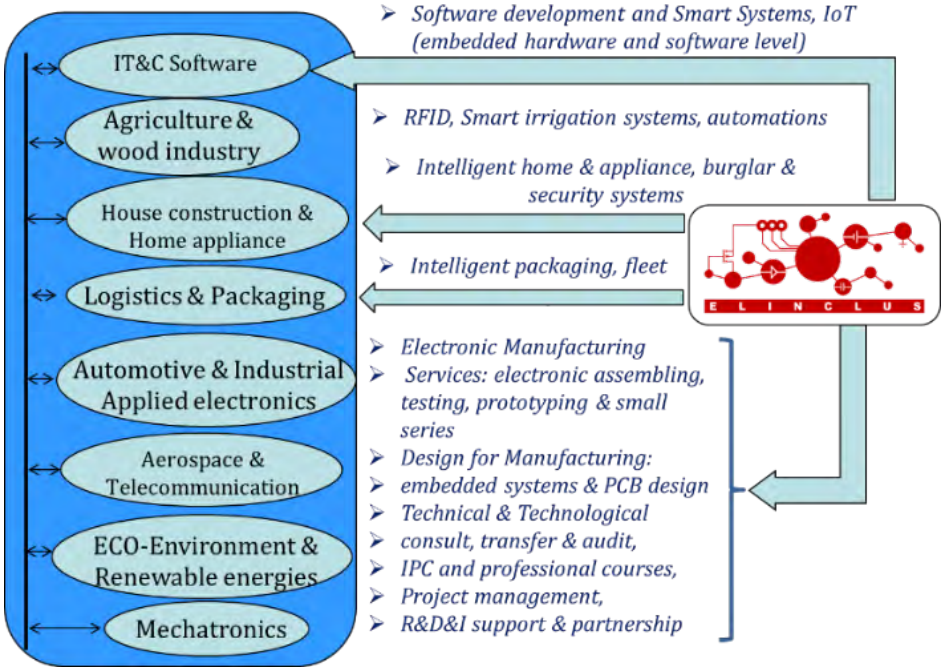
**EMC**: Association for Promoting Electronics Technology – APTE (www.apte.org.ro)

Founded 2011; 94 registered members

**President**: Prof. DHC. mult. Paul SVASTA,Ph.D.

**Executive Manager**: Lect. Eng. Bogdan Mihăilescu, Ph.D.

- Founding member of the Clusters Association from Romania, CLUSTERO - www.clustero.eu
- European Cluster Excellence Initiative Silver Label Certificate from ESCA since 2016
- Founding member of the IT Cluster Network from Romania comprised of 9 members 9: Transilvania IT Cluster, ALT – Brașov, Banat Software, Innovative Clsuter Open Hub, INOMAR, **ELINCLUS**, ICT Oltenia, ICT Cluster Lower Danube și Smart Alliance Cluster.
- Founding member of the regional Digital Innovation Hub – Smart e-Hub https://smartehub.eu/




• **E-mail**: office@elinclus.ro **Web page**: **www.elinclus.ro**

# ASSOCIATION FOR PROMOTING ELECTRONICS TECHNOLOGY (ASOCIAȚIA PENTRU PROMOVAREA TEHNOLOGIEI ELECTRONICE)

# IMAPS ROMANIA

A globally-competitive workforce with theoretical, as well as applied engineering/hands-on, education must be trained. In addition to the areas of science, engineering, microelectronics, and packaging, this training must encompass the broader areas of business, economics, ethics, foreign culture, and languages.

The Association for Promoting Electronics Technology (APTE, see https://apte.org.ro/) is IMAPS Romania. APTE was founded in 2002, by the Center for Technological Electronics and Interconnection Techniques (CETTI) together with highly respected members of the electronics industry, in order to support the electronics packaging education and engineering, in a climate of trust, ethics, and social responsibility.

APTE/IMAPS Romania is the management entity of the ELINCLUS Cluster (see http://elinclus.ro/), which has currently 94 members. ELINCLUS was established starting from the economic relationship existing between CETTI (which developed a Technological and Business Incubator, entity accredited by the National Innovation and Technology Transfer Network – ReNITT) and companies from Bucharest and Ilfov county. This structure has offered to ELINCLUS the status of a regional cluster in the field of electronics.

APTE offers annually a comprehensive set of short courses and training classes in the area of electronics packaging, IPC standards certification, management, and industrial development, in order to serve the needs of the electronics industry. APTE organises annually The International Symposium for Design and Technology in Electronics Packaging (SIITME, see http://siitme.ro/) and the Technologies of Interconnection in Electronics (TIE, see www.tie.ro/) Industry-Wide student challenges.

**Contact:**

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Phone: +40 21 4103108
E-mail: apte@apte.org.ro

ITEC Information Technology in Electronics Research Center

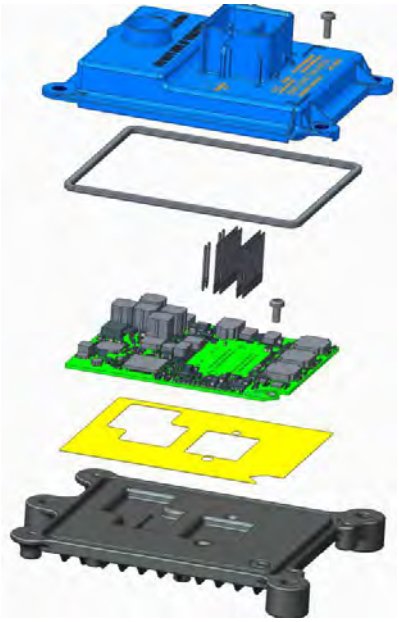
TECHNICAL UNIVERSITY OF CLUJ-NAPOCA ROMANIA

## ITEC Research Center

belongs to the Technical University of Cluj-Napoca having 25 researchers in Embedded Systems (electronics & software). ITEC can access the entire infrastructure of Technical University of Cluj-Napoca, resources from all other research centers and resources from Romanian University Alliance.

## ITEC Competencies

- Circuit design: modeling, simulation and cross-simulation of electronic circuits (analog, digital, power, RF/EMI) & system design: modeling and simulation for electro-mechanical systems: power devices, actuators, mechatronics;
- HW Application design: fast-prototype design, PCB design for mass production, BOM/AVL design, DfM & DfT for embedded applications, power supplies, interface/signal conditioning boards;
- SW Application design: embedded control applications for OS and non-OS targets;
- TW Application design: testing and design of testing systems: SW and HW testing process, HiL and SiL, design of test-cases for SW;
- Training services: LabVIEW trainings, Embedded Systems trainings, TW and HiL operation;
- PCB DESIGN: DfX, SI and PI.



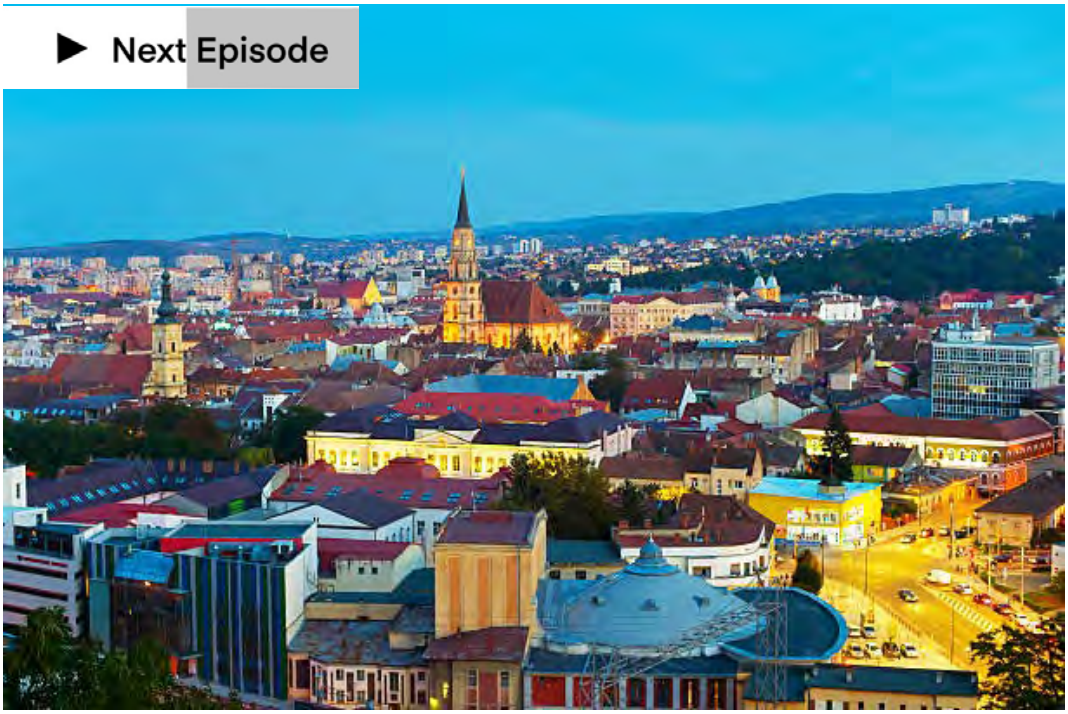
**Contact**

Information Technology in Electronics Research Center | Technical University of Cluj-Napoca
400027, G. Baritiu 26-28, Cluj-Napoca, Romania | E-Mail: gabriel.chindris@ael.utcluj.ro

# Welcome TIE 2026 - Technical University of Cluj-Napoca!

We are pleased to invite you to the 2026 edition of the Technologies of Interconnections in Electronics (TIE) Industry-Wide student challenges, to be held in Cluj-Napoca, Romania. TIE is an esteemed professional competition aimed at promoting technological computer-aided design (CAE-CAD-CAM) of electronic modules among students. Since its inception in 1992, TIE has brought together students and industry representatives to foster innovation and excellence in electronics design.

Cluj-Napoca, often referred to as the heart of Transylvania, is renowned for its vibrant cultural scene and historical significance. The city offers a perfect blend of rich history and modern innovation, making it an ideal setting for the TIE 2026 contest.




We look forward to welcoming you to Cluj-Napoca for TIE 2026, where you can showcase your skills, engage with peers and industry leaders, and experience the unique charm of this remarkable city!

**Local Organizing Chair:**

**Assoc. Prof. eng. Gabriel CHINDRIȘ, Ph.D.**

# Venue of the TIE 2025 & Microelectronics Day

**Events Location**:
Transilvania University of Brașov Library, Street Iuliu Maniu 41A, Brașov 500091

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